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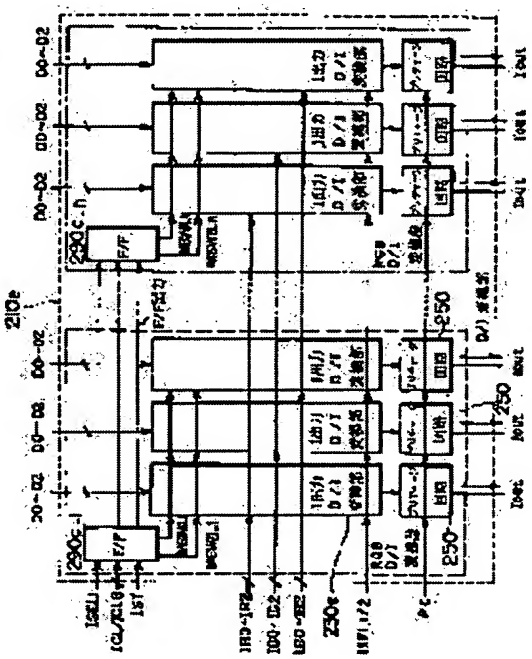
(54) SEMICONDUCTOR DEVICE FOR DRIVING CURRENT LOAD DEVICE AND CURRENT LOAD DEVICE EQUIPPED WITH THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To supply an output current with high precision for inputted digital image data and to drive a current load device fast even when the output current value is small.
SOLUTION: A D/I conversion part 210e of a semiconductor device for driving a light emission display device is provided with precharge circuits 250 behind respective 1-output D/I conversion parts 230e respectively. A precharge signal PC is inputted to each precharge circuit 250. Each D/I conversion part 230e has two output blocks inside and change the role of storing and outputting a current, frame by frame, to secure a long period for driving pixels. The precharge circuit 250 performs current driving after applying a voltage corresponding to the output current to the pixel, which can be driven at a high speed.



* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1]A semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device characterized by comprising the following.
A function to memorize a current value of n (n is natural number) kind determined by one sort or two or more sorts of reference current inputted.
A function which outputs one current according to n bit digital data inputted among current values of 2^n level obtained from said memory current value.

[Claim 2]The semiconductor device for a current load device drive according to claim 1, wherein said reference current is obtained by reference current generation circuit in said semiconductor device for a current load device drive.
[Claim 3]The semiconductor device for a current load device drive according to claim 1 or 2 provided with a circuit which transmits digital data which current does not output to said n bit digital / current conversion circuit at the time of said current memory, and transmits digital data which outputs current corresponding to operation of the purpose at the time of a current output.

[Claim 4]Said n bit digital / current conversion circuit memorize one sort of current values from one sort of reference current, A semiconductor device for a current load device drive given in any 1 paragraph of claims 1 thru/or 3 provided with n 1-bit digital / current conversion circuits which decide whether to output said memory current with 1 bit digital data inputted.
[Claim 5]The semiconductor device for a current load device drive according to claim 4, wherein said 1-bit digital / current conversion circuit memorize a current value of said reference current.

[Claim 6]A ratio of a current value of said n reference current is set as what was doubled one by one from the lowest current value, and said n bit digital current conversion circuit, By considering it as an output of said n bit digital / current conversion circuit, what connected an output of said n 1-bit digital / current conversion circuits in parallel. The semiconductor device for a current load device drive according to claim 4 or 5 characterized by the ability to output a current value of 2^n level according to n bit digital data.
[Claim 7]A semiconductor device for a current load device drive given in any 1 paragraph of claims 4 thru/or 6 characterized by comprising the following.
A signal wire in which said reference current flows through said 1-bit digital / current conversion circuit.
The data line with which 1 bit of said digital image data is transmitted.
The 1st and 2nd control lines.
The 1st and 2nd voltage supply lines and the 1st transistor by which sauce was connected to said 1st voltage supply line, A capacitative element connected between a gate of said transistor, and said 2nd voltage supply line, The 1st switch controlled by a signal which is connected between a drain of said 1st transistor, and said output terminal, and transmits said data line, The 2nd switch controlled by a signal which is connected between a gate of said 1st transistor, a drain of said 1st transistor, or said signal wire, and transmits said 2nd control line, The 3rd

switch controlled by a signal which is connected between a drain of said 1st transistor, and said signal wire, and transmits said 1st control line.

[Claim 8]A semiconductor device for a current load device drive given in any 1 paragraph of claims 4 thru/or 6 characterized by comprising the following.
A signal wire in which said reference current flows through said 1-bit digital / current conversion circuit.
The data line with which 1 bit of said digital image data is transmitted.
The control line.
The 1st and 2nd voltage supply lines and the 1st transistor by which sauce was connected to said 1st voltage supply line, A capacitative element connected between a gate of said 1st transistor, and said 2nd voltage supply line, The 1st switch controlled by a signal which is connected between a drain of said 1st transistor, and said output terminal, and transmits said data line, The 2nd switch controlled by a signal which is connected between a drain of a gate of said 1st transistor, and said transistor of 1, or said signal wire, and transmits said control line, The 3rd switch controlled by a signal which is connected between a drain of said transistor, and said signal wire, and transmits said control line.

[Claim 9]Between sauce of said 1st transistor, and said 1st voltage supply line, The semiconductor device for a current load device drive according to claim 7 or 8, wherein a gate is provided with said 1-bit digital / current conversion circuit which had the 2nd transistor by which bias is carried out with the 3rd voltage supply line added.
[Claim 10]When said 2nd and 3rd switches are ON states in an OFF state, said 1st switch said transistor, Voltage between gate sauce of said transistor in a stage which between the gate drain connected too hastily, operated in a saturation region, and was stabilized in the operation, It becomes voltage required in order to send said reference current between drain sauce, If the value will be determined according to current capability of said transistor, reference current according to current capability of said transistor will serve as voltage which flows between drain sauce and the 2nd and 3rd switches of an account of back to front will be in an OFF state, Voltage between gate sauce of said transistor is held at said capacitative element, A semiconductor device for a current load device drive given in any 1 paragraph of claims 7 thru/or 9 to which it is characterized by what is determined by operation of said 1st switch whether reference current based on voltage between this held gate sauce is outputted.
[Claim 11]The semiconductor device for a current load device drive according to claim 10, wherein said 3rd switch is turned off after said 2nd switch is turned off.
[Claim 12]A semiconductor device for a current load device drive given in any 1 paragraph of claims 7 thru/or 11, wherein a switch of said 1st [the] thru/or 3 comprises a transistor.
[Claim 13]An inversion signal of a signal inputted into a gate of a transistor where said 1-bit digital / current conversion circuit constitute said 2nd switch is inputted into a gate, A product of the length of a gate and width is 1/2 of a product of the length of a gate of a transistor and width which constitute said 2nd switch, The semiconductor device for a current load device drive according to claim 12 having the dummy transistors which a drain was connected to a gate of said 1st transistor, and sauce connected with a drain too hastily.
[Claim 14]Said n bit digital / current conversion circuit memorize two or more current values below n from said one sort inputted of reference current, So that the number of current values which digital one/current conversion circuit which decides whether to output said two or more memory current with digital data of the number of current values and a same number bit which were memorized memorized may be set to n, A semiconductor device for a current load device drive given in any 1 paragraph of claims 1 thru/or 3 characterized for said digital one/current conversion circuit by 1 or having more than one.
[Claim 15]The semiconductor device for a current load device drive according to claim 14, wherein one of two or more current values which said digital one/current conversion circuit memorize from one sort of reference current is said reference current value inputted.
[Claim 16]A ratio of each output current value of said n bit digital / current conversion circuit

constituted by 1, or two or more of said digital one/current conversion circuits, What is set as what was doubled one by one from the lowest current value, and connected an output in parallel by considering it as an output of said n bit digital / current conversion circuit. The semiconductor device for a current load device drive according to claim 14 or 15 characterized by the ability to output a current value of 2^n level according to n bit digital data.
[Claim 17]A semiconductor device for a current load device drive given in any 1 paragraph of claims 14 thru/or 16 characterized by comprising the following.
A signal wire in which said reference current flows through said digital one/current conversion circuit.
The data line of k (k is natural number below n) book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The control line, the 1st and 2nd voltage supply lines, and a transistor for current memory by which sauce was connected to said 1st voltage supply line, k transistors for current outputs which a gate short-circuits mutually and by which common connection of the sauce was carried out to the 1st voltage supply line, A capacitative element connected between a gate of said transistor for current outputs, and said 2nd voltage supply line, k switches for output controls controlled by either of the signals which is connected between a drain of said k transistors for current outputs, and said output terminal, respectively, and transmits said data line, The 1st switch for storage controls controlled by a signal which is connected between a drain of said transistor for current memory, and said signal wire, and transmits said control line, The 2nd switch for storage controls controlled by a signal which is connected between a gate of said transistor for current memory, and a gate of said transistor for current outputs, and transmits said control line.

[Claim 18]A semiconductor device for a current load device drive given in any 1 paragraph of claims 14 thru/or 16 characterized by comprising the following.
A signal wire in which said reference current flows through said digital one/current conversion circuit.
The data line of k book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The 1st and 2nd control lines, the 1st and 2nd voltage supply lines, and a transistor for current memory by which sauce was connected to said 1st voltage supply line, k transistors for current outputs which a gate short-circuits mutually and by which common connection of the sauce was carried out to the 1st voltage supply line, A capacitative element connected between a gate of said transistor for current outputs, and said 2nd voltage supply line, k switches for output controls controlled by either of the signals which is connected between a drain of said k transistors for current outputs, and said output terminal, respectively, and transmits said data line, The 1st switch for storage controls controlled by a signal which is connected between a drain of said transistor for current memory, and said signal wire, and transmits said 2nd control line, The 2nd switch for storage controls controlled by a signal which is connected between a gate of said transistor for current memory, and a gate of said transistor for current outputs, and transmits said 1st control line.

[Claim 19]A semiconductor device for a current load device drive given in any 1 paragraph of claims 14 thru/or 16 characterized by comprising the following.
A signal wire in which said reference current flows through said digital one/current conversion circuit.
The data line of k book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The control line, the 1st and 2nd voltage supply lines, and current memory and a transistor for an output, A gate connects with a gate of said current memory and a transistor for an output too hastily, and sauce k-1 transistor for current outputs, A capacitative element connected between a gate of said transistor for current outputs, and said 2nd voltage supply line, k switches for output controls controlled by either of the signals which is connected between a drain of said current memory and a transistor for an output, and k-1 transistor for current outputs, and said output terminal, respectively, and transmits said data line, The 1st switch for storage controls controlled by a signal which is connected between a drain of said

current memory and a transistor for an output, and said signal wire, and transmits said control line, The 2nd switch for storage controls controlled by a signal which is connected between a drain of said current memory, a gate of a transistor for an output and said current memory, and a transistor for an output, or a signal wire, and transmits said control line.

[Claim 20]A semiconductor device for a current load device drive given in any 1 paragraph of claims 14 thru/or 16 characterized by comprising the following.
A signal wire in which said reference current flows through said digital one/current conversion circuit.
The data line of k book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The 1st and 2nd control lines, the 1st and 2nd voltage supply lines, and current memory and a transistor for an output by which sauce was connected to said 1st voltage supply line, k-1 transistor for current outputs which a gate connects with a gate of said current memory and a transistor for an output too hastily and by which common connection of the sauce was carried out to the 1st voltage supply line, A capacitative element connected between a gate of said transistor for current outputs, and said 2nd voltage supply line, k switches for output controls controlled by either of the signals which is connected between a drain of said current memory and a transistor for an output, and k-1 transistor for current outputs, and said output terminal, respectively, and transmits said data line, The 1st switch for storage controls controlled by a signal which is connected between a drain of said current memory and a transistor for an output, and said signal wire, and transmits said 2nd control line, The 2nd switch for storage controls controlled by a signal which is connected between a drain of said current memory, a gate of a transistor for an output and said current memory, and a transistor for an output, or a signal wire, and transmits said 1st control line.

[Claim 21]A semiconductor device for a current load device drive given in any 1 paragraph of claims 17 thru/or 20 characterized by comprising the following.
Said object for current memory or current memory, and a transistor for an output.
Said 1-bit digital / current conversion circuit where a gate had two or more 2nd transistors by which bias is carried out with the 3rd voltage supply line added between each sauce of said transistor for an output, and said 1st voltage supply line

[Claim 22]A semiconductor device for a current load device drive given in any 1 paragraph of claims 17 thru/or 21, wherein current capability of said current memory and a transistor for an output is the same as a transistor with the highest current capability in said transistor for current outputs or is more than it.
[Claim 23]When the said 1st and 2nd switches for storage controls are ON states in the state of OFF of said switch for output controls, said transistor for current memory, Voltage between gate sauce of said transistor for current memory in a stage which between the gate drain connected too hastily, operated in a saturation region, and was stabilized in the operation, If it becomes voltage required in order to send said reference current between drain sauce, and the value is determined according to current capability of said transistor for current memory and the account 1st of back to front and the 2nd switch for storage controls are turned off, Voltage between gate sauce of said transistor for current memory is held at said capacitative element, Said n transistors for current outputs will be in the state where current of n kind can be sent with the total based on each current capability from reference current based on voltage between this held gate sauce, A semiconductor device for a current load device drive given in any 1 paragraph of claims 17 thru/or 22 to which it is characterized by what is determined by digital image data which is said n bit whether current which said transistor for current outputs can send is outputted.
[Claim 24]The semiconductor device for a current load device drive according to claim 23, wherein said 2nd switch for storage controls is turned off after said 1st switch for storage controls is turned off.
[Claim 25]A semiconductor device for a current load device drive given in any 1 paragraph of

claims 14 thru/or 24, wherein the said switch for output controls, 1st, and 2nd switches for storage controls comprise a transistor.
[Claim 26]Said digital one/current conversion circuit, Said 2nd control line. An inversion signal of a signal to transmit. Dummy transistors which were 1/2 of a product of the length of a gate of a transistor and width from which it is inputted into a gate and a product of the length of a gate and width constitutes said 1st switch for storage controls, and a drain was connected to a gate of said transistor for current memory, and sauce connected with a drain too hastily. The having semiconductor device for a current load device drive according to claim 25.
[Claim 27]Said n bit digital / current conversion circuit are the p bit digital / the current conversion circuit according to any one of claims 7 to 13, and the m bit digital according to any one of claims 17 to 26 / current conversion circuit (p and m are natural numbers.). A semiconductor device for a current load device drive constituting by p+m=n combining.
[Claim 28]A semiconductor device for a current load device drive given in claims 7 thru/or 13, wherein said 1st and 2nd power source wires are used as a common power source wire, and any 1 paragraph of 17 thru/or 27.
[Claim 29]A kind from which a relation of current of a current load device in a and said current load device and operation of the number of said n bit digital / current conversion circuits differs is b, and 1 or said two or more sorts of reference current, A semiconductor device for a current load device drive given in any 1 paragraph of claims 1 thru/or 28, wherein current storage operation which a thing corresponding to a current load device of b kind is prepared, respectively, and memorizes said reference current value is performed in an a/b step.
[Claim 30]In [a kind from which a relation of current of a current load device in those or more with two and said current load device and operation of a group whose number of said n bit digital / current conversion circuits is a differs is b, and] arbitrary frames, Make a certain group into a circuit for current outputs, and either of other groups is made into a circuit for current memory, A semiconductor device for a current load device drive given in any 1 paragraph of claims 1 thru/or 28 performing memory of current in an a/b step using the same reference current within each frame, and changing a role of a current output and current memory every [every frame or] several frames.
[Claim 31]A semiconductor device for a current load device drive given in any 1 paragraph of claims 1 thru/or 30, wherein a shift count which said storage operation has in said semiconductor device for a current load device drive is performed synchronizing with an output signal of a shift register more than an a/b bit.
[Claim 32]In a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device, have two or more current output circuits and a precharge circuit, and said precharge circuit, A semiconductor device for a current load device drive, wherein it is possible to supply voltage it is decided by output current of said current output circuit that will be a cell on said data line via the data line in said current load device, and to supply output current of said current output circuit as it is.
[Claim 33]The semiconductor device for a current load device drive according to claim 32 characterized by comprising the following.
A dummy load circuit which is load with said precharge circuit equivalent to load in a current load device driven according to output current from said current output circuit.
A voltage follower which carries out impedance conversion of the voltage produced when output current of said current output circuit is supplied to said dummy load, and outputs it.

[Claim 34]The semiconductor device for a current load device drive according to claim 33 using a dummy load circuit of said precharge circuit as load equivalent to a current load device or cell circuit load which holds and supplies current, and an equivalent circuit load.
[Claim 35]Voltage produced by supplying output current of said current output circuit to said dummy load circuit as precharge operation in early stages of one horizontal period, By a voltage follower in said precharge circuit, carry out impedance conversion and it goes via the data line of said current load device, It is impressed by a current load device or cell circuit load in a cell in said current load device, and as the aftercurrent drive operation, The semiconductor device for a

current load device drive according to claim 33 or 34 supplying output current of said current output circuit to a current load device or cell circuit load in a cell in said current load device directly via the data line of said current load device.
[Claim 36]A semiconductor device for a current load device drive given in any 1 paragraph of claims 33 thru/or 35, wherein said precharge circuit has the composition which cancels offset voltage of said voltage follower.
[Claim 37]The semiconductor device for a current load device drive according to claim 36 performing once operation which cancels offset voltage of a voltage follower in said precharge circuit to 1 or several frames.
[Claim 38]A semiconductor device for a current load device drive given in any 1 paragraph of claims 32 thru/or 37, wherein said current output circuits are the n bit digital / the current conversion circuit according to any one of claims 1 to 31.
[Claim 39]A semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device characterized by comprising the following.
Two or more n bit digital / current conversion circuits which memorize one or more reference current values, and output current according to n bit digital data
A shift register for current memory which outputs a scanning signal which synchronizes with storage operation of said reference current of said n bit digital / current conversion circuit performed one by one.
n bit data latch which transmits n bit digital data to n bit-data selector.
n bit-data selector which decides whether to transmit n bit digital data from said n bit data latch to n bit digital / current conversion circuit by whether operation to which said n bit digital / current conversion circuit output whether operation which memorizes said reference current is performed, and current is performed.

[Claim 40]The semiconductor device for a current load device drive according to claim 39 having a circuit which generates said reference current in a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device.
[Claim 41]The semiconductor device for a current load device drive according to claim 40, wherein said n bit digital / current conversion circuit are the n bit digital / the current conversion circuit according to any one of claims 1 to 31.
[Claim 42]A semiconductor device for a current load device drive given in any 1 paragraph of claims 39 thru/or 41 provided with a precharge circuit which performs precharge operation which outputs voltage in a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device before outputting current.
[Claim 43]The semiconductor device for a current load device drive according to claim 42, wherein said precharge circuit is a precharge circuit given in any 1 paragraph of claims 32 thru/or 38.
[Claim 44]In a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device, Operation holding n bit digital data inputted, and n bit data register outputted to said data latch, A semiconductor device for a current load device drive given in any 1 paragraph of claims 39 thru/or 43 having at least a shift register for data-hold which outputs a signal which synchronizes with maintenance operation of n bit digital data of said n bit data register performed one by one.
[Claim 45]A semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device characterized by comprising the following.
An output of said current output circuit or a precharge circuit.
An output selector which connects any one of two or more of the data lines of a current load device.

[Claim 46]By choosing two or more data lines one by one, and driving them in one horizontal period, by said output selector in a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device. The semiconductor device for a current load device drive according to claim 45 driving a current load device with

said current output circuits fewer than the number of the data lines, or the number of precharge circuits.
[Claim 47]A semiconductor device for a current load device drive given in any 1 paragraph of claims 1 thru/or 46 on which all the transistors were accumulated by one chip as a thin film transistor.
[Claim 48]A semiconductor device for a light-emitting display drive given in any 1 paragraph of claims 1 thru/or 47 in which said current load devices are light emitting devices.
[Claim 49]A semiconductor device for an organic electroluminescence display drive given in any 1 paragraph of claims 1 thru/or 47 in which said current load devices are organic EL devices.
[Claim 50]A current load device with which a semiconductor device for a current load device drive of a statement was created by any 1 paragraph of claims 1 thru/or 49 on the same substrate as a current load device.
[Claim 51]The current load device according to claim 50 provided with a semiconductor device for a current load device drive having load with the same composition and size as a cell circuit which holds and supplies said current load device or said current in each aforementioned current load cell as a dummy load in said precharge circuit.
[Claim 52]The current load device according to claim 50 or 51 provided with a semiconductor device for a current load device drive, wherein said current load device is a light emitting device.
[Claim 53]The current load device according to claim 50 or 51 provided with a semiconductor device for a current load device drive, wherein said current load device is an organic EL device.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention about the current load device provided with the semiconductor device for a current load device drive for driving a current load device provided with two or more cells having contained the current load device, and it, It is related with the current load device provided with the semiconductor device for a current load device drive and it which perform a gradation display with the current value to which especially a current load device is supplied.
[0002]
[Description of the Prior Art]it is current load device **** as which operation is determined by the current supplied -- the current load device which equips matrix form with two or more cells is developed. The application is a light-emitting display whose current load device is a light emitting device, for example.
It is the organic electroluminescence display in which the organic EL device is used as a light emitting device.

[0003]Hereafter, taking the case of a light-emitting display, it explains as a current load device. Drawing 35 shows the composition of a matrix type light-emitting display.
[0004]A display comprises the horizontal drive circuit 200, the vertical-scanning (drive) circuit 300, and the indicator 400. A gradation display is realized by adjusting the current which flows into the light emitting device in the one pixel display part 100 of the indicator 400. In the light emitting device as which luminosity is determined by various current, current and luminosity are in proportionality. The drive method of a light-emitting display is classified into simple matrix driving and an active-matrix drive according to combination with the current or voltage impressed from the composition, the horizontal drive circuit 200, and the vertical scanning circuit 300 of the one pixel display part 100.
[0005]Drawing 36 is a circuit diagram showing the composition of one pixel display part in the case of simple matrix driving. In the one pixel display part 101 in the case of simple matrix driving, the light emitting device 130 is connected between the control line 110 and the signal wire 120 on each intersection of the control line 110 and the signal wire 120. As shown in drawing 35, the control line 110 is driven by the vertical scanning circuit 300, and drives the signal wire 120 by the horizontal drive circuit 200.
[0006]And if current or voltage is outputted to the Lth signal wire 120 from the horizontal drive circuit 200 in the period which the control line 110 is chosen one by one by the vertical scanning circuit 300 for [every], and is scanning the Kth control line 110, The current which flows into the Kth line light emitting device of the Lth row is determined, and the light emitting device emits light by the intensity corresponding to the current. Then, if the scan of eye ** (K+1) watch is started, luminescence of the light emitting device of the Kth line will be ended.
[0007]Drawing 37 is a circuit diagram showing the composition of one pixel display part in an active-matrix drive. In the one pixel display part 102 in an active-matrix drive. On each intersection of the control line 110 and the signal wire 120, switch SW100 controlled by potential

of the control line 110 is connected to the signal wire 110, The gate of TFT(Thin Film Transistor: thin film transistor) T100 and one end of the capacitative element C100 are connected to the other end of switch SW100. The sauce of TFTT100 and the other end of the capacitative element C100 are grounded, and the light emitting device 130 is connected for the drain and potential of TFTT100 between the signal wires of VEL.

[0008]And if the control line 110 is chosen one by one by the vertical scanning circuit 300 for [every] and the Kth control line 110 is chosen, switch SW100 in the one pixel display part 102 will become one. At this time, the Lth output voltage of the horizontal drive circuit 200 turns into gate voltage of TFTT100, and the impedance of TFTT100 will be determined if the gate voltage that TFTT100 operates in a saturation region is impressed. As a result, the current which flows into the light emitting device 130 is determined, and the light emitting device 130 emits light by the intensity corresponding to that current.

[0009]In an active-matrix drive, one pixel display part may take other composition. Drawing 38 (a) and drawing 38 (b) are the circuit diagrams showing other composition of one pixel display part in an active-matrix drive. As shown in drawing 38 (a), in the one pixel display part 103 of other composition, switch SW102 controlled by potential of the control line 110 is connected to the signal wire 110, and the gate and drain of P channel TFTT102 are connected to the other end of switch SW102. Switch SW101 controlled by potential of the control line 110 is connected to this gate and drain, and the gate of P channel TFTT101 and one end of the capacitative element C100 are connected to that other end. The constant potential VEL is supplied to the sauce of TFTT101 and T102, and the other end of the capacitative element C100. The light emitting device 130 is connected between the drain of TFTT101, and earth-potentials GND.

[0010]And if the Kth control line 110 is chosen by the vertical scanning circuit 300 and the switches SW101 and SW102 serve as one, the gate voltage of TFTT102 will be decided so that the Lth output current of the horizontal drive circuit 200 may be sent from the signal wire 120. Since TFTT102 and TFTT101 have taken current mirror composition, when the current capability of TFTT102 and TFTT101 is mutually equal, It lets TFTT101 pass, the same current as the output current value of the horizontal drive circuit 200 flows into the light emitting device 130, and the light emitting device 130 emits light by the intensity according to the current value.

[0011]Same operation is performed also when N channels TFTT103 and T104 are used instead of P channels TFTT101 and T102, as shown in drawing 38 (b).

[0012]Since voltage is accumulated in the capacitative element also after the following line is chosen in an active-matrix drive if simple matrix driving is compared with an active-matrix drive, sending current can be continued. Therefore, compared with the case of the simple matrix driving of only emitting light momentarily, the current sent through a light emitting device becomes small.

[0013]Thus, even if the absolute values of current or voltage differ, in not being concerned with the kind of drive method of simple matrix driving and an active-matrix drive but performing a gradation display, the horizontal drive circuit 200 has the function to change digital gradation data into current or voltage. However, since dispersion in dispersion of the threshold of a transistor, the voltage-current characteristic of a light emitting device, and current-luminance property exists that it is a voltage output in a pixel circuit (one pixel display part), even if it impresses the same voltage, a possibility that luminosity varies is high. On the other hand, since it is influenced only by dispersion in the current-luminance property of a light emitting device in the case of a current output, the small and high-precision display of dispersion in luminosity is attained.

[0014]Drawing 39 is a block diagram showing an example of the composition of the horizontal drive circuit 200 for outputting current to the indicator 400. In this composition, after developing digital gradation data by the data logic section 201 in several output minutes, the current output for several output minutes is obtained in inputting those digital gradation data into digital ones / current conversion part 210.

[0015]Drawing 40 is a circuit diagram showing the 1st conventional example of digital one / current conversion part for one output. When gradation data is a triplet (D0 thru/or D2), common connection of switch SW110 controlled by these, respectively, SW111, and SW112 is carried out

to the outgoing end which outputs the current Idata. N channelTFTT110 and T111 by which input voltage VA is supplied to a gate, respectively, and T112 are connected between switch SW110, SW111, SW112, and the earthing conductor in the earth potentials VG. The current-luminance property of a light emitting device shall be in proportionality. The case where both the horizontal drive circuit 200 and the vertical scanning circuit 300 are formed on a glass substrate is assumed, and all transistors serve as TFT. Even when gradation data is more than a triplet, it is constituted similarly.

[0016]In the 1st conventional example, it is designed so that each channel length (L) may become fixed and the ratio of channel width (W) may be set to 1:2:4 about TFTT110, T111, and T112. In TFTT110 thru/or T112, since gate voltage serves as voltage VA and source voltage is all common with the voltage VG, when TFTT110 thru/or TT112 are operating in the saturation region, a current ratio is set to 1:2:4. Therefore, if suitable input voltage VA is chosen, the current output of 8 gradation used as 0-7 of a current ratio will become possible about the output current Idata by turning on and off the switches SW110 thru/or SW112 based on the gradation data D0 thru/or D2. The absolute value of current can be adjusted by changing input voltage VA.

[0017]Drawing 41 is a circuit diagram showing the 2nd conventional example of digital ones / current conversion part for one output. In the 2nd conventional example, the digital gradation data D0 thru/or D2 is inputted into the gate of N channels TFTT110 thru/or T112. Common connection of the drain of TFTT110 thru/or T112 is carried out to an outgoing end, and the power supply voltage VD is supplied to sauce. The ratio of the channel width of TFTT110 thru/or T112 is set as 1:2:4 like the 1st conventional example.

[0018]By considering it as the level which sets the high level of the digital-gradation-data input as suitable voltage beforehand and with which a thin film transistor turns off a low level in such 2nd conventional example instead of forming a switch. The current output of 8 gradation used as 0-7 of a current ratio becomes possible like the 1st conventional example. The absolute value of current can be adjusted by changing the high level of a digital-gradation-data input.

[0019]

[Problem(s) to be Solved by the Invention]However, in a transistor, especially TFT, since dispersion in current capability when the same gate voltage is impressed between different TFT (s) is large, there is a problem that it is difficult to take out a high-precision current output. In the conventional digital one / current conversion part, if there is characteristic dispersion of TFT throughout current load device width mostly, even if the size of TFT is uniform and the voltage between gate sauce is uniform, since a current value differs from other fields, display unevenness will occur in the scattered portion. If the characteristic of TFT which will be used for the output same in display unevenness occurring between adjacent pixels if current capability varies and the dispersion becomes large also between TFT(s) which are in a proximity region varies, it stops also satisfying the monotonicity of gradation.

[0020]In especially the conventional digital one / current conversion part, in an active-matrix drive, when an output current value is low, there is also a problem that a drive takes time. If the active-matrix drive by current drive is adopted, when the same current as the output current of digital one / current conversion part which is a drive circuit flows into TFT in a pixel, a drive will complete this, but. It is because it is necessary to carry out the charge and discharge of those volume loads by the output current which is constant current since wiring load, especially parasitic capacitance certainly exist in the signal wire 110 in the indicator 400 and a light emitting device also has capacity value in it. That is, since the same current as the output current of digital one/current conversion circuit which is a drive circuit flows into TFT in a pixel only after carrying out the charge and discharge of those capacity to a certain voltage, it takes long time by then.

[0021]This invention was made in view of this problem, and is ****. The purpose can supply high-precision output current to **** digital image data, It is providing the light-emitting display provided with the semiconductor device for a light-emitting display drive and it which can drive a light-emitting display at high speed, even when [desirable] an output current value's is low, and providing the current load device provided with still more general semiconductor device for a

current load device drive and it.

[0022]
[Means for Solving the Problem]A semiconductor device for a current load device drive concerning this invention, In a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device, A function to memorize a current value of n (n is natural number) kind determined by one sort or two or more sorts of reference current inputted, It has at least one n bit digital / current conversion circuit provided with a function which outputs one current according to n bit digital data inputted among current values of 2^n level obtained from said memory current value for every supply terminal to said one or more cells.
[0023]Other semiconductor devices for a current load device drive concerning this invention, In a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device, have two or more current output circuits and a precharge circuit, and said precharge circuit, It is characterized by it being possible to supply voltage it is decided by output current of said current output circuit that will be a cell on said data line via the data line in said current load device, and to supply output current of said current output circuit as it is.
[0024]Furthermore it starts this invention, others a semiconductor device for a current load device drive, In a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device, Two or more n bit digital / current conversion circuits which memorize one or more reference current values, and output current according to n bit digital data, A shift register for current memory which outputs a scanning signal which synchronizes with storage operation of said reference current of said n bit digital / current conversion circuit performed one by one, n bit data latch which transmits n bit digital data to n bit-data selector, and said n bit digital / current conversion circuit by whether operation which memorizes said reference current is performed, or operation which outputs current is performed. It has at least n bit-data selector which decides whether to transmit n bit digital data from said n bit data latch to n bit digital / current conversion circuit.
[0025]And the composition is as follows when this invention is applied to a semiconductor device for a light-emitting display drive, or a light-emitting display.
[0026]Namely, the 1st semiconductor device for a light-emitting display drive concerning this invention, In a semiconductor device for a light-emitting display drive with which a light emitting device it is decided with current supplied that luminosity will be drives a light-emitting display provided in each pixel, A reference current value for 1 bit. n 1-bit digital / current conversion circuits to memorize. To 1, or two or more 1-bit digital / current conversion circuits which each preparation inputted reference current of n kind corresponding to the current-luminance property of said light emitting device memorized in said one 1-bit digital / current conversion circuit, and were chosen based on digital image data of n bit, said reference current. It is set as what has n bit digital / current conversion circuit which outputs current of 2^n kind for every output terminal which outputs current to said light-emitting display, and doubled it one by one to a current value with the respectively lowest current value of said n kind of reference current by making it output.
[0027]Said 1-bit digital / current conversion circuit, A signal wire in which said reference current flows, and the data line with which 1 bit of said digital image data is transmitted, The control line, the 1st and 2nd voltage supply lines, and the 1st transistor by which sauce was connected to said 1st voltage supply line, A capacitative element connected between a gate of said 1st transistor, and said 2nd voltage supply line, The 1st switch controlled by a signal which is connected between a drain of said 1st transistor, and said output terminal, and transmits said data line, The 2nd switch controlled by a signal which is connected between drains of a gate of said 1st transistor, said signal wire, or said 1st transistor, and transmits said control line, The 3rd switch controlled by a signal which is connected between a drain of said 1st transistor, and said signal wire, and transmits said control line, A signal wire in which it may **** and said reference

current flows, the data line with which 1 bit of said digital image data is transmitted, the 1st and 2nd control lines, the 1st and 2nd voltage supply lines, and the 1st transistor by which sauce was connected to said 1st voltage supply line, A capacitative element connected between a gate of said 1st transistor, and said 2nd voltage supply line, The 1st switch controlled by a signal which is connected between a drain of said 1st transistor, and said output terminal, and transmits said data line, The 2nd switch controlled by a signal which is connected between drains of a gate of said 1st transistor, said signal wire, or said 1st transistor, and transmits said 2nd control line, It may have the 3rd switch controlled by a signal which is connected between a drain of said 1st transistor, and said signal wire, and transmits said 1st control line.

[0028]Or a gate may have the 2nd transistor by which bias was carried out between said 1st transistor and said 1st voltage supply line.

[0029]When said 2nd and 3rd switches are ON states in an OFF state, said 1st switch said transistor, Voltage between gate sauce of said transistor in a stage which between the gate drain connected too hastily, operated in a saturation region, and was stabilized in the operation, If it becomes voltage required in order to send said reference current between drain sauce, and the value will be determined according to current capability of said transistor and the 2nd and 3rd switches of an account of back to front will be in an OFF state, If it is determined by operation of said 1st switch whether voltage between gate sauce of said transistor is held at said capacitative element, and reference current based on voltage between this held gate sauce is outputted, Since each output has said n 1-bit digital / current conversion circuits, according to said n bit digital image data, current of 2^n level according to the current-luminance property of said light emitting device can be outputted. Therefore, said 1-bit digital / current conversion circuit cannot be concerned with current capability dispersion of a transistor which memorizes and outputs said current, but can output current of high accuracy.

[0030]Since influence of a noise by OFF operation of a transistor as said 3rd switch will become small if said 3rd switch is turned off after said 2nd switch is turned off, Said 1-bit digital / current conversion circuit can memorize and output current more at high degree of accuracy.

[0031]Said 1st [the] thru/or the 3rd switch may comprise a transistor.

[0032]To said 1-bit digital / current conversion circuit. Said 2nd control line. Dummy transistors which were 1/2 of a product of the length of a gate of a transistor and width from which an inversion signal of a signal to transmit is inputted into a gate, and a product of the length of a gate and width constitutes said 2nd switch, and a drain was connected to a gate of said transistor and sauce connected with a drain too hastily. Since movement of an electric charge at the time of a transistor as said 2nd switch turning off by providing can be compensated, as for said 1-bit digital / current conversion circuit, current can be memorized and outputted more at high degree of accuracy.

[0033]In this invention, in current storage duration, the 1st transistor that memorizes n current in n bit each digital / current conversion circuit short-circuits between gate drains, it is operating in a saturation region, and voltage between gate sauce is the voltage into which reference current stabilizes and flows. At the time of an end of current storage duration, a switch which has short-circuited between gate drains is turned off, and voltage between said gate sauce is saved in capacity. It is holding voltage between gate sauce which is not concerned with current capability dispersion of said 1st n transistor, but sends reference current in order to memorize voltage between gate sauce through which said 1st n transistor sends reference current according to each current capability at this time, and current is memorized. In a driving period, the 1st transistor that memorized said n current, It decides whether output memorized current by turning on and off n switches between each drain of the 1st transistor that memorized said n current, and an output of said digital one/current conversion circuit according to image digital data. Since current outputted in this way is outputted from the transistor itself which memorized said n current, it becomes a thing without influence of current capability dispersion which has high accuracy. By the above operations, n bit digital / current conversion circuit of this invention become possible [outputting current with high accuracy from which a current ratio becomes 0, 1, 2, ..., 2^{n-1}]. In this case, in order to constitute n bit digital / current

conversion circuit, n reference current sources are needed.
[0034]When said gate has the 2nd transistor by which bias was carried out, Cascode connection is made, and said 1st transistor and the 2nd transistor can stop dispersion in current supplied, even if the characteristic of a light emitting device varies, since the drain voltage dependency of drain current can be suppressed when operating in both saturation regions.
[0035]The 2nd semiconductor device for a light-emitting display drive concerning this invention, In a semiconductor device for a light-emitting display drive with which a light emitting device it is decided with current supplied that luminosity will be drives a light-emitting display provided in each pixel, Memorize one sort of reference current values, and current of 2^n kind corresponding to the current-luminance property of said light emitting device is generated from said memorized reference current based on digital image data of n bit. It has n bit digital / current conversion circuit to output for every output terminal which outputs current to said light-emitting display.
[0036]Said n bit digital / current conversion circuit, A signal wire in which said reference current flows, and the data line of n book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The control line, the 1st and 2nd voltage supply lines, and a transistor for current memory by which sauce was connected to said 1st voltage supply line, n transistors for current outputs which a gate short-circuits mutually and by which common connection of the sauce was carried out to the 1st voltage supply line, A capacitative element connected between a gate of said transistor for current outputs, and said 2nd voltage supply line, n switches for output controls controlled by either of the signals which is connected between a drain of said n transistors for current outputs, and said output terminal, respectively, and transmits said data line, The 1st switch for storage controls controlled by a signal which is connected between a drain of said transistor for current memory, and said signal wire, and transmits said control line, The 2nd switch for storage controls controlled by a signal which is connected between a gate of said transistor for current memory, and a gate of said transistor for current outputs, and transmits said control line, It **** and current capability of said n transistors for current outputs may be set as what was doubled one by one to the respectively lowest current capability, A signal wire in which said reference current flows through n bit digital / current conversion circuit, The data line of n book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The 1st and 2nd control lines, the 1st and 2nd voltage supply lines, and a transistor for current memory by which sauce was connected to said 1st voltage supply line, n transistors for current outputs which a gate short-circuits mutually and by which common connection of the sauce was carried out to the 1st voltage supply line, A capacitative element connected between a gate of said transistor for current outputs, and said 2nd voltage supply line, n switches for output controls controlled by either of the signals which is connected between a drain of said n transistors for current outputs, and said output terminal, respectively, and transmits said data line, The 1st switch for storage controls controlled by a signal which is connected between a drain of said transistor for current memory, and said signal wire, and transmits said 2nd control line, Have the 2nd switch for storage controls controlled by a signal which is connected between a gate of said transistor for current memory, and a gate of said transistor for current outputs, and transmits said 1st control line, and current capability of said n transistors for current outputs, It may be set as what was doubled one by one to the respectively lowest current capability.
[0037]Or a gate may have the bias transistor by which bias was carried out, respectively between said transistor for current memory, said transistor for current outputs, and said 1st voltage supply line.
[0038]When the said 1st and 2nd switches for storage controls are ON states in the state of OFF of said switch for output controls, said transistor for current memory, Voltage between gate sauce of said transistor for current memory in a stage which between the gate drain connected too hastily, operated in a saturation region, and was stabilized in the operation, If it becomes voltage required in order to send said reference current between drain sauce, and the value is determined according to current capability of said transistor for current memory and the account 1st of back to front and the 2nd switch for storage controls are turned off, Voltage between gate

sauce of said transistor for current memory is held at said capacitative element, Said n transistors for current outputs will be in the state where current of n kind can be sent with the total based on each current capability from reference current based on voltage between this held gate sauce, It may be determined by digital image data whether whose current which said transistor for current outputs can send is outputted it is said n bit.
[0039]As for said 2nd switch for storage controls, it is preferred to be turned off, after said 1st switch for storage controls is turned off.
[0040]The said switch for output controls, 1st, and 2nd switches for storage controls may comprise a transistor.
[0041]Said n bit digital / current conversion circuit, Said 2nd control line. An inversion signal of a signal to transmit. Dummy transistors which were 1/2 of a product of the length of a gate of a transistor and width from which it is inputted into a gate and a product of the length of a gate and width constitutes said 1st switch for storage controls, and a drain was connected to a gate of said transistor for current memory, and sauce connected with a drain too hastily. Having is preferred.
[0042]This invention can be used when current capability dispersion of a transistor in a proximity region is small. A transistor which memorizes current in said n bit digital / current conversion circuit memorizes current by the same means as the 1st semiconductor device concerning above-mentioned this invention. They are a transistor which memorizes said current, a transistor which outputs said current, and current mirror composition here, A current capability ratio is 1:2:4. : ... Current capability most a current capability ratio with a large transistor among n transistors for an output which are :2 $^{n-1}$ like 1:1 or 2:1, If a transistor which memorizes current is made equally or large, a reference current value becomes large, and since a period which carries out the charge and discharge of the wiring load in which reference current flows is shortened, current storage duration can be shortened. Since a transistor which memorizes said current at this time memorizes gate source voltage in the state where reference current flowed, it is not based on dispersion in current capability, but can memorize current in high accuracy. Therefore, when current capability dispersion of a transistor in a proximity region is small, By having as a means, n switches switch on and off according to digital input image data between a drain of said transistor for an output, and an output of said n bit digital / current conversion circuit. A current ratio becomes possible [outputting current with high accuracy used as 0, 1, 2, ..., 2^{n-1}]. n bit digital / current conversion circuit can be constituted from one reference current source in this case, and a required input can be lessened.
[0043]When said gate has here the bias transistor by which bias was carried out, Said transistor for current memory, said transistor for current outputs, and said bias transistor, Cascode connection is made, and since the drain voltage dependency of drain current can be suppressed when operating in both saturation regions, even if the characteristic of a light emitting device varies, dispersion in current supplied can be stopped.
[0044]The 3rd semiconductor device for a light-emitting display drive concerning this invention, In a semiconductor device for a light-emitting display drive with which a light emitting device it is decided with current supplied that luminosity will be drives a light-emitting display provided in each pixel, Reference current of k kind corresponding to the current-luminance property of said light emitting device. Memorize and current of a seed from said memorized k kind of reference current (n-k). It has n bit digital / current conversion circuit which generates and outputs current of a 2 ^{n} kind based on digital image data of n bit from combination of these current for every output terminal which outputs current to said light-emitting display.
[0045]Said n bit digital / current conversion circuit, A signal wire of k book with which said reference current flows, and the data line of n book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The control line, the 1st and 2nd voltage supply lines, and k transistors for a current memory output by which sauce was connected to said 1st voltage supply line, A transistor for current outputs of an individual (n-k) which a gate connected with any one of said k transistors for a current memory output too hastily, 1 or two or more capacitative elements which were connected between a gate of said transistor for a current

memory output, and said 2nd voltage supply line, n switches for output controls controlled by either of the signals which is connected between a drain of said transistor for a current memory output, and said transistor for current outputs, and an output terminal, respectively, and transmits said data line, The 1st k switch for storage controls controlled by a signal which is connected between a drain of said transistor for a current memory output, and said signal wire, and transmits said control line, Have the 2nd k switch for storage controls controlled by a signal which is connected between a gate of said transistor for a current memory output, and a drain, and transmits said control line, and current capability of each of said transistor for current outputs, Rather than that of said all transistors for a current memory output, it is low and current capability of said transistor for current outputs, and said transistor for a current memory output, It may be set as what was doubled one by one to the respectively lowest current capability, and said n bit digital / current conversion circuit, A signal wire of k book with which said reference current flows, and the data line of n book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The 1st and 2nd control lines, the 1st and 2nd voltage supply lines, and k transistors for a current memory output by which sauce was connected to said 1st voltage supply line, A transistor for current outputs of an individual (n-k) which a gate connected with any one of said k transistors for a current memory output too hastily, 1 or two or more capacitative elements which were connected between a gate of said transistor for a current memory output, and said 2nd voltage supply line, n switches for output controls controlled by either of the signals which is connected between a drain of said transistor for a current memory output, and said transistor for current outputs, and an output terminal, respectively, and transmits said data line, The 1st k switch for storage controls controlled by a signal which is connected between a drain of said transistor for a current memory output, and said signal wire, and transmits said 2nd control line, The 2nd k switch for storage controls controlled by a signal which is connected between a gate of said transistor for a current memory output, and a drain, and transmits said 1st control line, It ****, and current capability of each of said transistor for current outputs is lower than that of said all transistors for a current memory output, and current capability of said transistor for current outputs and said transistor for a current memory output may be set as what was doubled one by one to the respectively lowest current capability.

[0046]Or a gate may have the bias transistor by which bias was carried out, respectively between said transistor for current memory, said transistor for current outputs, and said 1st voltage supply line.

[0047]When said switch for output controls is [the said 1st and 2nd switches for storage controls] ON states in an OFF state, said transistor for a current memory output, Voltage between gate sauce of said transistor for a current memory output in a stage which between the gate drain connected too hastily, operated in a saturation region, and was stabilized in the operation, If it becomes voltage required in order to send said reference current between drain sauce, and the value is determined according to current capability of said current and a transistor for a memory output and the account 1st of back to front and the 2nd switch for storage controls are turned off, Voltage between gate sauce of said transistor for a current memory output is held at said capacitative element, A transistor for said transistor for current outputs, current memory, and an output will be in the state where current of n kind can be sent with the total based on each current capability from reference current based on voltage between this held gate sauce, It may be determined by digital image data whether whose current which said transistor for current outputs and a transistor for a current memory output can send is outputted it is said n bit.

[0048]As for said 2nd switch for storage controls, it is preferred to be turned off, after said 1st switch for storage controls is turned off.

[0049]The said switch for output controls, 1st, and 2nd switches for storage controls may comprise a transistor.

[0050]Said n bit digital / current conversion circuit, Said 2nd control line. An inversion signal of a signal to transmit. Dummy transistors which were 1/2 of a product of the length of a gate of a transistor and width from which it is inputted into a gate and a product of the length of a gate

and width constitutes said 1st switch for storage controls, and a drain was connected to a gate of said current memory and a transistor for an output, and sauce connected with a drain too hastily. Having is preferred.

[0051]This invention can be used when current capability dispersion of a transistor in a proximity region is a little small. In current storage duration, 1 in n bit digital / current conversion circuit means thru/or said some of current memory, and a transistor for an output memorize reference current of a transistor and the same number by the same means as ****. Therefore, 1 which memorizes said current - some transistors can output current of high accuracy. On the other hand, a transistor which memorizes and outputs said current, and 1 which is current mirror composition - some transistors for an output are making it output current lower than said reference current, and even when current capability varies, they can make influence in the whole small. By the above composition, a current ratio is 1:2:4. : ... Current which is :2^{n-1} can be supplied in high accuracy, By having as a means, n switches which turn on and off said current according to digital input image data between a drain of a transistor memorized and outputted or said transistor for an output, and an output of said digital one/current conversion circuit. A current ratio becomes possible [outputting current with high accuracy used as 0, 1, 2, ..., 2^{n-1}]. Digital one/current conversion circuit can be constituted from 1 thru/or some reference current sources in this case, and an input from the outside can be lessened.

[0052]When said gate has here the bias transistor by which bias was carried out, Said transistor for current memory, said transistor for current outputs, and said bias transistor, Cascode connection is made, and since the drain voltage dependency of drain current can be suppressed when operating in both saturation regions, even if the characteristic of a light emitting device varies, dispersion in current supplied can be stopped.

[0053]This invention can constitute n bit digital / current conversion circuit means combining digital one / current conversion circuit means of above-mentioned either of the 1st to 3. By for example, a thing for which bit (n-1) digital / current conversion circuit of the 2nd invention in a bit not more than it are used for a bit with the highest current value using said 1-bit digital / current conversion circuit of the 1st invention. While accuracy of a large bit with the highest current value of influence of dispersion is high, reference current can constitute n bit digital / current conversion circuit whose number is two.

[0054]In this invention, said 1st and 2nd voltage supply lines may be used as a common power source wire.

[0055]When the luminescent color whose number of said output terminals is a pixel of a and said light-emitting display is a b color, nx b sorts of reference current values are needed again, but. Because digital one/current conversion circuit which current storage operation may be performed in an a/b step, and is equivalent to one output at this time have said two n bit digital / current conversion circuits. In arbitrary frames, it is more preferred that make one side into a circuit for current outputs, make another side into a circuit for current memory, memory of current is performed in an a/b step using the same reference current within each frame, and a role of a current output and current memory is replaced for every frame. By replacing a frame rate for every frame, a period for memorizing current other than a period which drives a light-emitting display is not needed. Therefore, a period to drive can be considered to be the whole frame period, and can take one long horizontal period which drives one line, and it becomes possible to drive highly precise current to a pixel circuit. Above-mentioned operation is the same even when digital one/current conversion circuit equivalent to said one output are provided with said three or more n bit digital / current conversion circuits for example. Every multiple frame may replace a role of a current output and current memory.

[0056]This invention has a precharge circuit which outputs suitable voltage in current outputted from a current output circuit like said n bit digital / current conversion circuit being inputted, A dummy load circuit which said precharge circuit will serve as load equivalent to said light emitting device if said light-emitting display is a simple matrix type, and will serve as load equivalent to a pixel circuit if said light-emitting display is an active matrix system, A voltage follower which considers voltage when output current from said current output circuit flows into said dummy

load circuit as an input, The 1st switch for precharge connected between an output of said current output circuit, and said dummy load circuit, The 1st control line for precharge that transmits a signal which controls said 1st switch for precharge, The 2nd switch for precharge that connects an output and said light-emitting display of said current output circuit, The 2nd control line for precharge that transmits an inversion signal of a signal which controls said 2nd switch for precharge and controls said 1st switch for precharge, It is preferred to have the 3rd switch controlled by a signal which is connected between an output of said voltage follower and said light-emitting display, and transmits said 1st control line for precharge.

[0057]Output current of said current output circuit is supplied to said dummy load circuit as precharge operation in early stages of one horizontal period, The voltage is impressed to a light emitting device or said pixel circuit in said pixel in said light-emitting display via a voltage follower, By supplying output current of said current output circuit to a light emitting device or said pixel circuit in said pixel in said light-emitting display directly as the aftercurrent drive operation, Since time for charge and discharge can shorten wiring load in said light-emitting display, etc. even when output current of said current output circuit is small, a light emitting device or said pixel circuit in said pixel in said light-emitting display can be driven more to stability and a high speed, and high degree of accuracy.

[0058]By providing again composition which cancels offset voltage of said voltage follower in said precharge circuit, By performing operation which cancels offset voltage of said voltage follower at the time of said current drive operation. Since a difference at the time of supplying a pixel (circuit) in a case where output current of a circuit which excessive time is unnecessary, and also memorizes and outputs said current is supplied to said dummy load circuit, and said actual light-emitting display becomes small, A light emitting device or said pixel circuit in said pixel in said light-emitting display can be driven more to stability and a high speed, and high degree of accuracy.

[0059]Since said false pixel (circuit) is near said the digital one/current conversion circuit by providing a precharge circuit, even when wiring load in the meantime is small and current outputted is small, said false pixel (circuit) comes to send outputted current stably in short time. Input into a voltage follower gate voltage in the state where current is flowing into said false pixel (circuit) stably, and an output of said voltage follower by connecting with the data line of a light-emitting display. Voltage with output current of said current output circuit near voltage in the state where it is flowing into a pixel (circuit) in said indicator stably is impressed to a pixel (circuit) in said signal wire or said indicator. The above precharge operation can perform load of said data line at high speed compared with carrying out charge and discharge by constant current. After voltage of a pixel (circuit) in said data line and said indicator is stabilized by precharge operation, said false pixel (circuit) is separated from said current output circuit, and current is outputted to said data line directly from said current output circuit. In this case, charge and discharge of load of said data line by constant current which is an output of said current output circuit, or a pixel (circuit) in said indicator, Since precharge has already been performed, what is necessary is just to carry out slightly, and it is not influenced by load of said signal wire before precharge, voltage of a pixel (circuit) in said indicator, etc. Driving time can be shortened. Therefore, it becomes possible stability and to carry out the current drive of the pixel (circuit) at high speed and with high precision, without being influenced by performing two steps of above drive operation by voltage of wiring load of light-emitting display circles before a drive, or load of a pixel (circuit).

[0060]A semiconductor device for a light-emitting display drive concerning this invention, For every output, memorize reference current and said n bit digital / current conversion circuit which outputs current of 2^n kind according to n bit digital data One or more preparations, And by whether said n bit digital / current conversion circuit perform an output or storage operation of current. It has a data selector which performs whether data from n bit data latch and said n bit data latch is transmitted to said n bit digital / current conversion circuit, and has a shift register for current memory which outputs a scanning signal which synchronized with operation which memorizes said reference current as the whole device further. Said semiconductor device

for a light-emitting display drive has said precharge circuit for every output again. Said semiconductor device for a light-emitting display drive is provided with n bit data register which holds n bit digital data which is inputted from the outside, and which is inputted synchronizing with a scanning signal of a shift register for data-hold for every output, and is provided with said shift register for data-hold as the whole device. By what it has further an output selector circuit connectable [in one horizontal period / an output of said n bit digital / current circuit, or said precharge circuit] with two or more data lines of a light-emitting display one by one according to selector signals for. Said semiconductor device for a light-emitting display drive can drive a light-emitting display by less circuit structure.

[0061]One chip may be accumulated with a circuit which generates said reference current. A transistor may comprise a thin film transistor.

[0062]It has one which was accumulated by one chip with a circuit which a light-emitting display concerning this invention is formed in the same substrate as said light emitting device, and generates said reference current of the above-mentioned semiconductor devices for a light-emitting display drive.

[0063]When said light emitting device and a semiconductor device for a light-emitting display drive are especially formed in the same substrate, since dummy load (circuit) in said precharge circuit can be constituted from same size as load (circuit) in a pixel of a display, and shape, it can make accuracy of precharge voltage obtained high. At this time, the driving method which combined above-mentioned precharge operation and current output operation can be driven more to stability, a high speed, and high degree of accuracy.

[0064]A semiconductor device for a light-emitting display drive and a light-emitting display of this invention are applicable also to a semiconductor device and a current load device for driving a more common current load device and a current load device which comprise a current load device instead of as above-mentioned. [a light emitting device]

[0065]

[Embodiment of the Invention]The semiconductor device for light-emitting displays is taken for an example like ****, and the semiconductor device for current load devices concerning the example of this invention is concretely explained with reference to an attached drawing. In attaching and showing an underbar and a number when an order is set up by the same component, and observing separately, it shows the following explanation, without attaching an underbar and a number.

[0066]Drawing 1 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 1st example of this invention. Digital one / current (D/I) converter 210 is formed in the 1st example, The shift register which comprised the n flip-flops (F/F) 290_1 thru/or 290_n provided in this D/I converter 210 every 1 output D/I converters 230 for the number of outputs to a light-emitting display (3xn) and three outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, and the inversion signal ICLB of this clock signal ICL are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230, and either the reference current IR0 thru/or IR2 for referring to it, IG0 to IG2, IB0 to IB2 are inputted into it according to the luminescent color assigned to it. Reference current is the current value whose luminescent color suited to red and the current-luminance property of each blue and green light emitting device, current value irof reference current IR00 -- the luminescent color -- a red light emitting device -- corresponding to eyes 1 gradation -- current value irof reference current IR11 -- the luminescent color -- a red light emitting device -- corresponding to eyes 2 gradation -- current value irof reference current IR22 -- the luminescent color -- red -- it corresponds to eyes 4 gradation. the same -- 1 gradation whose luminescent color of the current value of the reference current IG0 thru/or IG2 is green respectively -- eyes and 2 gradation -- eyes -- corresponding to eyes 4 gradation -- 1 gradation of blue [reference current / IB0 thru/or IB2 / luminescent color] respectively -- eyes and 2 gradation -- eyes -- it corresponds to eyes 4 gradation. The one RGB D/I converter 220 comprises the three 1 output D/I converters 230 into which signal municipal solid waste outputted from one F/F290 and this F/F290 is inputted.

[0067]Drawing 2 is a block diagram showing the composition of the 1 output D/I converter 230. The 1 output D/I converter 230 comprises the three 1-bit D/I converters 231. In these 1-bit D/I converters 231, respectively The image data D0 and the combination of the reference current I0, Either of the combination of the combination of the image data D1 and the reference current I1, the image data D2, and the reference current I2 is inputted, and signal municipal solid waste which is an output signal of F/F is inputted. The reference current I0 thru/or I2 corresponds to the combination of the reference current IR0 thru/or IR2, the combination of the reference current IG0 thru/or IG2, or combination of the reference current IB0 thru/or IB2. That is, in the 1 output D/I converter 230 for a red (R) display, the reference current supplied to the 1-bit D/I converter 231 into which the digital gradation data D0 is inputted is reference current IR0 corresponding to the luminosity of eyes 1 gradation of the light emitting device for red displays. The reference current supplied to the 1-bit D/I converter 231 into which the digital gradation data D1 is inputted, It is reference current IR1 corresponding to the luminosity of eyes 2 gradation of the light emitting device for red displays, and the reference current supplied to the 1-bit D/I converter 231 into which the digital gradation data D2 is inputted is reference current IR2 corresponding to the luminosity of eyes 4 gradation of the light emitting device for red displays. However, since the current-luminance property of a light emitting device has proportionality, the relation between ir1=2xir0 and ir2=4xir0 is realized. Similarly it is the 1-bit D/I converter 231 provided in the object for the green (G) display, or the 1 output D/I converter 230 for a blue (B) display, Reference current IG0 or IB0, reference current IG1 or IB1, reference current IG2, or IB2 are inputted into that into which the gradation data D0, D1, and D2 are inputted, respectively.

[0068]Drawing 3 is a block diagram showing the composition of the 1-bit D/I converter 231. The transistor N channel thin film transistor (TFT) T1, the switches SW1 thru/or SW3, and the capacitative element C1 for current memory / output are provided in the 1-bit D/I converter 231. It is connected to the drain of TFTT1 and switch SW1 is controlled by gradation data D*. The output current Iout is outputted from the other end of switch SW1. It is connected between the point of contact with the switches SW1 and TFTT1, and the end of the capacitative element C1 and the gate of TFTT1, and switch SW2 is controlled by signal municipal solid waste. One end of switch SW3 is connected to the signal wire in which reference current I* is supplied, it is connected between the point of contact with the switches SW1 and TFTT1, and one end of the capacitative element C1, and the other end is controlled by signal municipal solid waste. Although the sauce of TFTT1 and the other end of the capacitative element C1 are grounded, for example, when there is no operation top problem, voltage higher than ground voltage GND may be supplied.Gradation data D* and reference current I* are equivalent to either the gradation data D0 and the reference current I0, the gradation data D1 and the reference current I1, the gradation data D2 and the reference current I2.

[0069]Next, operation of the semiconductor device for light-emitting displays concerning the 1st example constituted as mentioned above is explained. Drawing 4 is a timing chart which shows operation of the semiconductor device for light-emitting displays concerning the 1st example of this invention. Y_1 in drawing 4, and Y_2, respectively The 1st line of the vertical scanning circuit 300 (refer to drawing 35), The output signal of the 2nd line is shown and D0, D1, and D2 show triplet digital image data (gradation data), Iout shows the output signal of the 1 output D/I converter 230, and IST shows the start signal of the shift register which comprises the n flip-flops 290, ICL shows the clock signal of a shift register and municipal solid waste_1 and municipal solid waste_2 show the output signal of the 1st step of a shift register, and the 2nd step, respectively.

[0070]Since it begins to carry out the vertical scanning of the indicator 400 (refer to drawing 35), the period until the next vertical scanning starts is made into one frame. One frame comprises a current driving period (the 1st operation period) and current storage duration (the 2nd operation period).

[0071]First, current storage duration (the 2nd operation period) is explained. In current storage duration, the 1-bit each D/I converter 231 memorizes the reference current supplied to each from the reference current source. Here, in this period, all the digital gradation data is made into

a low level, and switch SW1 of the 1-bit D/I converter 231 is off.
[0072]With the start of current storage duration, a pulse signal is inputted into F/F 290_1 of the 1st step as the start signal IST, Simultaneously with the input of this pulse signal, the shift register which comprises n F/F290 begins to operate in the clock signal ICL and the clock inversion signal ICLB being inputted into F/F 290_1. If output signal municipal solid waste_1 of F/F 290_1 of the 1st step becomes high-level, the switches SW2 and SW3 of the 1-bit each D/I converter 231 provided in the 1 output D/I converter 230 into which this output signal municipal solid waste_1 is inputted will serve as one. If the switches SW2 and SW3 are turned on, since between the gate drain short-circuits, TFTT1 for current memory / output in the 1-bit D/I converter 231 will operate in a saturation region. And where this operation is stabilized, according to the current capability of TFTT1, the gate voltage is set up so that the reference current from a reference current source may flow between the drain sauce of TFTT1.
[0073]If signal municipal solid waste_1 is set to a low level and output signal municipal solid waste_2 of F/F of the 2nd step becomes high-level after being in a stable state, the switches SW2 and SW3 of the 1-bit each D/I converter 231 in the RGB D/I converter 220 in which F/F 290_1 was formed will be come by off. At this time, the gate voltage of TFTT1 in the RGBD/I converter 220 in which F/F 290_1 was formed is held at the voltage that reference current flows by the capacitative element C1. As a result, it is not concerned with each current capability, but reference current is memorized by TFTT1. Such a signal municipal solid waste makes a high-level period 3 output-current storage duration in the RGB D/I converter 220. On the other hand, each switches SW2 and SW3 in the RGB D/I converter 220 in which F/F of the 2nd step was provided serve as one, and in the state where it was stabilized. It operates in a saturation region so that reference current may flow between the drain sauce of TFTT1, and according to the current capability of TFTT1, gate voltage is set up so that the reference current may flow.
[0074]In current storage duration, the above 3 output-current storage duration is repeated about all the RGB D/I converters 220, and reference current is memorized by all the 1 output D/I converters 230.
[0075]Next, a current driving period (the 1st operation period) is explained. In the current driving period, the vertical scanning circuit 300 chooses the control line (scanning line) of one line at a time. The scanning pulse Y_1 which is the 1st line and 2nd-line output, and Y_2 are shown in drawing 4.
[0076]If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1 output D/I converter 230 for every output synchronizing with this. If the digital gradation data D0 thru/or D2 is inputted, according to these levels (the high level (H) / low level (L)), ON and OFF of switch SW1 in the 1-bit D/I converter 231 will be controlled, and the current memorized by TFTT1 in the current driving period of the last frame will be outputted. The relation between the input digital gradation data D0 thru/or D2 and gradation (output current value) is shown in the following table 1.
[0077]
[Table 1]

階調	階調データ			出力電流値 (Ｉｏｕｔの電流値)
	Ｄ０	Ｄ１	Ｄ２	
0	Ｌ	Ｌ	Ｌ	0
1	Ｈ	Ｌ	Ｌ	ｉ０
2	Ｌ	Ｈ	Ｌ	ｉ１＝２×ｉ０
3	Ｈ	Ｈ	Ｌ	ｉ１＋ｉ０＝３×ｉ０
4	Ｌ	Ｌ	Ｈ	ｉ２＝４×ｉ０
5	Ｈ	Ｌ	Ｈ	ｉ２＋ｉ０＝５×ｉ０
6	Ｌ	Ｈ	Ｈ	ｉ２＋ｉ１＝６×ｉ０
7	Ｈ	Ｈ	Ｈ	ｉ２＋ｉ１＋ｉ０＝７×ｉ０

[0078]As shown in Table 1, an output current value can be adjusted with the digital gradation data inputted from 0 to 7xi0. Since gate voltage is set up so that current equivalent to a reference current source may flow according to the current capability of TFTT1 by current storage duration (the 2nd operation period), and current is outputted using the TFTT1 [same], Regardless of dispersion in current capability, dispersion in output current is small and high accuracy is obtained.
[0079]On the other hand, in a current driving period (the 1st operation period), the shift register does not operate but all the switches SW2 and SW3 are still OFF always.
[0080]And by repeating the above operations about each frame, in the indicator 400, the display according to the gradation data D0 thru/or D2 is performed, and highly precise current is supplied to a pixel circuit in that case.
[0081]According to such 1st example, current can be supplied in a high speed and high accuracy to the light-emitting display which has P channel TFT as shown in drawing 38 (a).
[0082]Next, the 2nd example of this invention is described. The 2nd example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (b). Drawing 5 is a block diagram showing the composition of the 1-bit D/I converter in the 2nd example of this invention.
[0083]Instead of N channel TFTT1 in the 1st example, P channel TFTT2 is provided in the 1-bit D/I converter 231a in the 2nd example, and the power supply potential VD is supplied to the end of the sauce and the capacitative element C1. The voltage VD is comparable as the voltage VEL, or is low voltage, and let it be a level which does not have a problem in operation.
[0084]The 1st example can be applied when the transistor which sends the current of a pixel circuit as shown in drawing 38 (a) is P channel TFT, but the 2nd example is applicable to N channel TFT as shown in drawing 38 (b). That is, when TFT in a pixel circuit is P channel TFT, the source voltage is the voltage VEL, but when it is considered as N channel TFT, it is necessary to set the source voltage to ground level GND, and this example can respond to this.
[0085]Except for operation of the 2nd example changing the polarity of output current, it is the same as that of the 1st example, and the same effect is acquired.

[0086]Next, the 3rd example of this invention is described. The 3rd example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (a). Drawing 6 is a block diagram showing the composition of the 1-bit D/I converter in the 3rd example of this invention.
[0087]In the 1-bit D/I converter 231b in the 3rd example, not earth-potentials GND but suitable stable voltage VB is supplied to the end of the capacitative element C1.
[0088]Operation of the 3rd example is the same as that of the 1st example, and the same effect is acquired. The voltage by which this is supplied to the capacitative element C1 shows that what kind of voltage may be sufficient, if stabilized.
[0089]Next, the 4th example of this invention is described. The 4th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (b). Drawing 7 is a block diagram showing the composition of the 1-bit D/I converter in the 4th example of this invention.
[0090]In the 1-bit D/I converter 231c in the 4th example, not earth-potentials GND but suitable stable voltage VB is supplied to the end of the capacitative element C1 like the 3rd example. Like the 2nd example, P channel TFTT2 is provided instead of N channel TFTT1 in the 1st example, and the power supply potential VD is supplied to the end of the sauce and the capacitative element C1.
[0091]Thus, the 4th example is what applied the 3rd example to the 2nd example, and like the 3rd example, the voltage supplied to the capacitative element C1 shows that what kind of voltage may be sufficient, if stabilized.
[0092]Next, the 5th example of this invention is described. The 5th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (a). Drawing 8 is a block diagram showing the composition of the 1-bit D/I converter in the 5th example of this invention.
[0093]Instead of the switches SW1 thru/or SW3 in the 1st example, the N channel transistors T11 thru/or T13 are formed in the 1-bit D/I converter 231d in the 5th example, respectively.
[0094]Also by such 5th example, based on the timing chart shown in drawing 4, the same operation as the 1st example is performed, and the same effect is acquired. P channel transistor can also be used instead of the N channel transistors T11 thru/or T13. In this case, the timing chart should just reverse what shows drawing 4 the output signal of F/F.
[0095]Next, the 6th example of this invention is described. The 6th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (b). Drawing 9 is a block diagram showing the composition of the 1-bit D/I converter in the 6th example of this invention.
[0096]Instead of the switches SW1 thru/or SW3 in the 2nd example, the N channel transistors T11 thru/or T13 are formed in the 1-bit D/I converter 231e in the 6th example, respectively.
[0097]Also by such 6th example, based on the timing chart shown in drawing 4, the same operation as the 2nd example is performed, and the same effect is acquired. P channel transistor can also be used instead of the N channel transistors T11 thru/or T13. In this case, the timing chart should just reverse what shows drawing 4 the output signal of F/F.
[0098]Next, the 7th example of this invention is described. The 7th example is applied to the pixel circuit shown, for example in drawing 38 (a). Drawing 10 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 7th example of this invention.
[0099]The D/I converter 210a is formed in the 7th example, and to this D/I converter 210a. The shift register which comprised n flip-flop (F/F) 290a_1 thru/or 290 a_n which were provided every 1 output D/I converters 230a for the number of outputs to a light-emitting display (3xn) and three outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, the inversion signal ICLB of this clock signal ICL, and current memory timing signal IT are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230a, and either the reference current IR0 thru/or IR2 for referring to it, IG0 to IG2, IB0 to IB2 are inputted into it according to the luminescent color assigned to it. The one RGB D/I converter 220a comprises the three 1 output

D/I converters 230a into which the signals municipal solid waste1 and municipal solid waste2 outputted from one F/F 290a and this F/F 290a are inputted.

[0100]Drawing 11 is a block diagram showing the composition of the 1 output D/I converter 230a. The 1 output D/I converter 230a comprises the three 1-bit D/I converters 231f. In these 1-bit D/I converters 231f. Either of the combination of the combination of the combination of the image data D0 and the reference current I0, the image data D1, and the reference current I1, the image data D2, and the reference current I2 is inputted, respectively, and the signals municipal solid waste1 and municipal solid waste2 which are output signals of F/F are inputted.

[0101]Drawing 12 is a block diagram showing the composition of the 1-bit D/I converter 231f. Transistor N channelTFTT1, the N channel transistors T11 thru/or T13, and the capacitative element C1 for current memory / output are provided in the 1-bit D/I converter 231f like the 5th example. Gradation data D0 and signal municipal solid waste2 and signal municipal solid waste1 are inputted into the gate of the transistor T11, T12, and T13, respectively, and each transistor is controlled by these signals.

[0102]Next, operation of the semiconductor device for light-emitting displays concerning the 7th example constituted as mentioned above is explained. Drawing 13 is a timing chart which shows operation of the semiconductor device for light-emitting displays concerning the 7th example of this invention.

[0103]In this example, as shown in drawing 13, in current storage duration, signal municipal solid waste1 changes like signal municipal solid waste in the 1st example. Current memory timing signal IT rises synchronizing with the standup of one of signal municipal solid waste1, and falls from the signal municipal solid waste1 to early timing. And signal municipal solid waste2 rises to the same timing as signal municipal solid waste1, and it falls synchronizing with falling of current memory timing signal IT. Let the period when signal municipal solid waste2 has risen be 3 output-current storage duration in the RGB D/I converter 220a.

[0104]In such 7th example, only the transistor T12 turns off the 1-bit D/I converter 231f at the time of the end of 3 output-current storage duration, and the transistor T13 turns it off after that. Therefore, the gate voltage of TFTT1 in the state where reference current is stably sent between drain sauce is not influenced by the noise at the time of the transistor T13 turning off, but is held more correctly. For this reason, this example can supply still higher-precision current as compared with the 5th example.

[0105]Next, the 8th example of this invention is described. The 8th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 7th example, for example, is shown in drawing 38 (b). Drawing 14 is a block diagram showing the composition of the 1-bit D/I converter in the 8th example of this invention.

[0106]P channel TFTT2 is provided for N channel TFTT1 in the 7th example in the 1-bit D/I converter 231g in the 8th example instead, and the power supply potential VD is supplied to the end of the sauce and the capacitative element C1.

[0107]Except for operation of the 8th example changing the polarity of output current, it is the same as that of the 7th example, and the same effect is acquired. For example, still higher-precision current can be supplied as compared with the 6th example.

[0108]Next, the 9th example of this invention is described. The 9th example is applied to the pixel circuit shown, for example in drawing 38 (a). Drawing 15 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 9th example of this invention.

[0109]The D/I converter 210b is formed in the 9th example, and to this D/I converter 210b. The shift register which comprised n flip-flop (F/F) 290b_1 thru/or 290 b_n which were provided every 1 output D/I converters 230b for the number of outputs to a light-emitting display (3xn) and three outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, the inversion signal ICLB of this clock signal ICL, and current memory timing signal IT are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230b, and either the reference current IR0 thru/or IR2 for referring to it, IG0 to IG2, IB0 to IB2 are inputted into it according to the luminescent color assigned to it. The one RGB D/I converter 220b comprises the three 1 output

D/I converters 230b into which signal municipal solid waste1 outputted from one F/F 290b and this F/F 290b, municipal solid waste2, and municipal solid waste2B are inputted. Signal municipal solid waste2B is an inversion signal of signal municipal solid waste2.

[0110]Drawing 16 is a block diagram showing the composition of the 1 output D/I converter 230b. The 1 output D/I converter 230b comprises the three 1-bit D/I converters 231h. In these 1-bit D/I converters 231h. Either of the combination of the combination of the combination of the image data D0 and the reference current I0, the image data D1, and the reference current I1, the image data D2, and the reference current I2 is inputted, respectively, and signal municipal solid waste1 which is an output signal of F/F, municipal solid waste2, and municipal solid waste2B are inputted.

[0111]Drawing 17 is a block diagram showing the composition of the 1-bit D/I converter 231h. Transistor N channelTFTT1, the N channel transistors T11 thru/or T13, and the capacitative element C1 for current memory / output are provided in the 1-bit D/I converter 231h like the 7th example. Gradation data D0 and signal municipal solid waste2 and signal municipal solid waste1 are inputted into the gate of the transistor T11, T12, and T13, respectively, and each transistor is controlled by these signals. In this example, the N channel transistor T14 is connected between the N channel transistor T12 and the end of the capacitative element C1. The sauce and the drain of the N channel transistor 14 are short-circuited mutually, and signal municipal solid waste2B is inputted into the gate. And the gate of TFTT1 is connected to the point of contact of the drain of the N channel transistor 14, and the end of the capacitative element C1. The transistor length L of the transistor T14 and the product with the transistor width W are the halves of the transistor length L of the transistor T12, and a product with the transistor width W.

[0112]The semiconductor device for light-emitting displays concerning the 9th example constituted in this way operates like the 7th example based on the timing chart shown in drawing 13. However, the waveform of signal municipal solid waste2B reverses the waveform of signal municipal solid waste2.

[0113]Therefore, while the transistor T12 turns off the 1-bit D/I converter 231h at the time of the end of 3 output-current storage duration, and the transistor T13 turns it off later than this. [the converter] [the transistor T14] For this reason, the gate voltage of TFTT1 in the state where reference current is stably sent between drain sauce, Movement of the electric charge produced when it is not influenced by the noise at the time of the transistor T13 turning off and the transistor T12 turns off is also absorbed by one of the transistor T14, and is held much more correctly. Thus, this example can supply still higher-precision current as compared with the 7th example.

[0114]Next, the 10th example of this invention is described. The 10th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 9th example, for example, is shown in drawing 38 (b). Drawing 18 is a block diagram showing the composition of the 1-bit D/I converter in the 10th example of this invention.

[0115]P channel TFTT2 is provided for N channel TFTT1 in the 9th example in the 1-bit D/I converter 231i in the 10th example instead, and the power supply potential VD is supplied to the end of the sauce and the capacitative element C1.

[0116]Except for operation of the 10th example changing the polarity of output current, it is the same as that of the 9th example, and the same effect is acquired. For example, still higher-precision current can be supplied as compared with the 8th example.

[0117]Next, the 11th example of this invention is described. The 11th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (a). Drawing 30 is a block diagram showing the composition of the 1-bit D/I converter in the 11th example of this invention.

[0118]In the 1-bit D/I converter 231j in the 11th example, it is not connected to the point of contact of the switches SW1 and TFT1, and the gate of TFTT1, but the both ends of SW2 are connected with the signal wire in which reference current I* is supplied at the gate of TFTT1, respectively.

[0119]Operation of the 11th example is the same as that of the 1st example, and the same

effect is acquired. The 2nd to the 1st example is performed and a change like the 10th example can be made.

[0120]Next, the 12th example of this invention is described. The 12th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (a). Drawing 31 is a block diagram showing the composition of the 1-bit D/I converter in the 12th example of this invention.

[0121]In the 1-bit D/I converter 231k in the 12th example, TFTT15 is added between TFTT1 and line GND and voltage VS1 [suitable] is impressed to the gate of TFT15.

[0122]Operation of the 12th example is the same as that of the 1st example, and the same effect is acquired. Since cascode connection of the TFTT15 and TFTT1 which were added is made, flattening of the drain voltage dependency of the drain current in the saturation region of TFT1 is carried out, and an example becomes possible [raising the accuracy of the output current Iout]. The 2nd [as opposed to the 1st example for being carried out] is performed, and this example can make a change like the 10th example.

[0123]Next, the 13th example of this invention is described. The 11th example is applied to the pixel circuit shown, for example in drawing 38 (a), and when current capability dispersion of a proximity region is small, it can be used. Drawing 19 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 13th example of this invention.

[0124]The D/I converter 210c is formed in the 13th example, and to this D/I converter 210c. The shift register which comprised the n flip-flops (F/F) 290_1 thru/or 290_n provided every the 1 output D/I converter 230c for the number of outputs to a light-emitting display (3xn) and 3 outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, and the inversion signal ICLB of this clock signal ICL are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230c, and IBreference current IR2 for referring to it, IG2, or 2 is inputted into it according to the luminescent color assigned to it. The one RGB D/I converter 220c comprises the three 1 output D/I converters 230c into which signal municipal solid waste outputted from one F/F290 and this F/F290 is inputted.

[0125]The luminescent color has doubled the current value of reference current with red and each blue and green current luminance property, current value irof reference current IR22 -- the luminescent color -- red -- it corresponds to eyes 4 gradation and current value igof reference current IG22 has the green luminescent color -- corresponding to eyes 4 gradation -- current value ibof reference current IB22 -- the luminescent color -- blue -- eyes are supported 4 gradation. That is, the reference current supplied to the 1 output D/I converter 230c for a red (R) display is reference current IR2 corresponding to the luminosity of eyes 4 gradation of the light emitting device for red displays. However, since the current-luminance property of a light emitting device has proportionality, it will be set to ir2=4xir0 if the current value corresponding to eyes is set to ir0 1 gradation. Similarly, reference current IG2 or IB2 are inputted into the object for the green (G) display, or the 1 output D/I converter 230c for a blue (B) display, respectively. Therefore, in this example, the minimum of the reference current inputted will be 4 times the 1st example. The reason for having made reference current correspond to eyes 4 gradation, It is because the current capability of N channel TFTT23 which memorizes the current provided in the 1 output D/I converter 230c like the after-mentioned, and the current capability of N channel TFTT22 which outputs the current which is equivalent to eyes 4 gradation were designed become equal.

[0126]Drawing 20 is a block diagram showing the composition of the 1 output D/I converter 230c. Switch SW23a by which it is controlled by signal municipal solid waste, and reference current I* is supplied to the end is provided in the 1 output D/I converter 230c. Common connection of the drain and gate of N channel TFTT23 is carried out to the other end of the switch 23a. The sauce of TFTT23 is grounded. One end of switch SW23b controlled by signal municipal solid waste is connected to the drain and gate of N channel TFTT23, and common connection of the gate of N channels TFTT20 thru/or T22 and the one end of the capacitative element C2 is carried out to the other end at them. The sauce of TFTT20 thru/or T22 and the

other end of the capacitative element C2 are grounded. The gradation data D0, D1, switch SW20 that are controlled by D2, SW21, and SW22 are connected to the drain of TFTT20, T21, and T22, respectively, and common connection of the other end of these switches SW20 thru/or SW22 is carried out. The output current Iout is outputted from this common node. The current capability ratio of TFTT20, T21, and T22 is 1:2:4. The current capability of TFTT22 and the current capability of TFTT23 are designed become the same mutually. When there is no operation top problem, voltage higher than earth-potentials GND instead of earth-potentials GND may be supplied to the sauce of TFTT20 thru/or T23, and the end of the capacitative element C2. For example, it may be connected to the signal wire in which only the capacitative elements C2 differ.

[0127]The semiconductor device for light-emitting displays concerning the 13th example constituted in this way operates like the 1st example based on the timing chart shown in drawing 4.

[0128]In the current storage duration (the 2nd operation period) in the 13th example, the one output each D/I converter 230c memorizes the reference current (either IR2, IG2 or IB2) supplied to each from the reference current source. Here, in this period, all the digital gradation data is made into a low level, and the switches SW20 thru/or SW22 of the 1 output D/I converter 230c are off.

[0129]With the start of current storage duration, a pulse signal is inputted into F/F 290_1 of the 1st step as the start signal IST, Simultaneously with the input of this pulse signal, the shift register which comprises n F/F290 begins to operate in the clock signal ICL and the clock inversion signal ICLB being inputted into F/F 290_1. If output signal municipal solid waste_1 of F/F 290_1 of the 1st step becomes high-level, switch SW23a and SW23b which are provided in the 1 output D/I converter 230c in the RGB D/I converter 220c in which this F/F 290_1 is formed will become one. If switch SW23a and SW23b become one, since between the gate drain short-circuits, TFTT23 for current memory of the 1 output D/I converter 230c will operate in a saturation region. Then, if it will be in a stable state, according to the current capability of TFTT23, the gate voltage will be set up so that the reference current from a reference current source may flow between the drain sauce of TFTT23.

[0130]After being in a stable state, signal municipal solid waste_1 is set to a low level, and. If output signal municipal solid waste_2 of F/F of the 2nd step becomes high-level, switch SW23a and SW23b of the 1 output D/I converter 230c in the RGB D/I converter 220c in which F/F 290_1 was formed will be come by off. At this time, the voltage that TFTT23 sends reference current is held by the capacitative element C2 of the 1 output D/I converter 230c in the RGB D/I converter 220c in which F/F 290_1 was formed. Since the end of the capacitative element C2 is connected to the gate for [TFTT20 thru/or T22] an output, the objects TFTT20 thru/or T22 for an output, Corresponding to each current capability ratio to TFTT23, the current corresponding to eyes, the current corresponding to eyes 2 gradation, and the current corresponding to eyes 4 gradation can be sent 1 gradation, respectively. Such a signal municipal solid waste makes a high-level period 3 output-current storage duration in the RGB D/I converter 220c. On the other hand, switch SW23a and SW23b in the RGB D/I converter 220c in which F/F of the 2nd step was provided become one, and in the state where it was stabilized. It operates in a saturation region so that reference current may flow between the drain sauce of TFTT23, and according to the current capability of TFTT23, gate voltage is set up so that the reference current may flow.

[0131]In current storage duration, the above 3 output-current storage duration is repeated about all the RGB D/I converters 220c, and reference current is memorized by all the 1 output D/I converters 230c.

[0132]In the current driving period (the 1st operation period), the vertical scanning circuit 300 chooses the control line of one line at a time.

[0133]If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1 output D/I converter 230c for every output synchronizing with this. If the digital gradation data D0 thru/or D2 is inputted, according to these levels (the high level (H) /

low level (L)), ON and OFF of the switches SW20 thru/or SW22 will be controlled, The current memorized in the current driving period of the last frame is outputted according to the current capability of every TFTT20 thru/or T22. As a result, gray scale representation as shown in Table 1 becomes possible. Therefore, an output current value can be adjusted with the digital gradation data inputted from 0 to 7xi0. Since reference current is memorized according to dispersion in current capability by current storage duration (the 2nd operation period) and dispersion in current capability is small in a proximity region, regardless of current capability dispersion in a big field, current dispersion is small and high accuracy is obtained.

[0134]On the other hand, in a current driving period (the 1st operation period), the shift register does not operate but all the switch SW23a and SW23b are still OFF always.

[0135]And by repeating the above operations about each frame, in the indicator 400, the display according to the gradation data D0 thru/or D2 is performed, and highly precise current is supplied to a pixel circuit in that case.

[0136]According to such 13th example, since reference current is 4 times the minimum value of the reference current in the 1st example, the charge and discharge of the load of the wiring which sends reference current can be performed at high speed, and it can be quickly made a stable state. Therefore, since current storage duration can be shortened and a current driving period can be lengthened, still higher-precision current can be supplied to the pixel in an indicator.

[0137]Like the 2nd thru/or the 12th example to the 13th example, In composition as a pixel circuit shows drawing 38 (b), the polarity of a transistor may be changed, A transistor may be used as a switch and output current accuracy may be raised by adding shifting mutually the timing of OFF of switch SW23a and SW23b, and a transistor. The minimum value of reference current can be enlarged more by making current capability of TFTT23 larger than the current capability of TFTT22, for example. In this case, since current storage duration can be shortened and a current driving period can be lengthened, charge and discharge time, such as load which wiring to the pixel in an indicator has, can be secured now for a long time, and the current of still higher accuracy can be supplied to a pixel.

[0138]Next, the 14th example of this invention is described. The 14th example is applied to the pixel circuit which changes the composition of the 1 output D/I converter in the 13th example, for example, is shown in drawing 38 (a), and when current capability dispersion of a proximity region is a little small, it can be used. Drawing 21 is a block diagram showing the composition of the 1-bit D/I converter in the 14th example of this invention.

[0139]In the 1 output D/I converter 230d in the 14th example, TFTT23 is not provided but the end of switch SW23a is connected to the drain of TFTT22. Switch SW23b is connected between the drain of TFTT22, and sauce.

[0140]Like the 13th example, the current value of reference current, the luminescent color has doubled with red and each blue and green current luminance property -- current value irof reference current IR22 -- the luminescent color -- red -- it corresponds to eyes 4 gradation and current value igof reference current IG22 has the green luminescent color -- corresponding to eyes 4 gradation -- current value ibof reference current IB22 -- the luminescent color -- blue -- eyes are supported 4 gradation. That is, the reference current supplied to the 1 output D/I converter 230d for a red (R) display is reference current IR2 corresponding to the luminosity of eyes 4 gradation of the light emitting device for red displays. However, since the current-luminance property of a light emitting device has proportionality, it will be set to ir2=4xir0 if the current value corresponding to eyes is set to ir0 1 gradation. Similarly, reference current IG2 or IB2 are inputted into the object for the green (G) display, or the 1 output D/I converter 230c for a blue (B) display, respectively. Therefore, in this example, the minimum of the reference current inputted will be 4 times the 1st example. The reason for having made reference current correspond to eyes 4 gradation is because the current capability of TFTT20 for an output of the 1 output D/I converter 230d and T21 and the current capability of TFTT22 which memorizes and outputs current were designed like the after-mentioned so that it might be set to 1:2:4.

[0141]The semiconductor device for light-emitting displays concerning the 14th example constituted in this way as well as the 1st example operates based on the timing chart shown in

drawing 4.

[0142]In the current storage duration (the 2nd operation period) in the 14th example, the one output each D/I converter 230d memorizes the reference current (either IR2, IG2 or IB2) supplied to each from the reference current source. Here, in this period, all the digital gradation data is made into a low level, and the switches SW20 thru/or SW22 of the 1 output D/I converter 230d are off.

[0143]With the start of current storage duration, a pulse signal is inputted into F/F 290_1 of the 1st step as the start signal IST, Simultaneously with the input of this pulse signal, the shift register which comprises n F/F290 begins to operate in the clock signal ICL and the clock inversion signal ICLB being inputted into F/F 290_1. If output signal municipal solid waste_1 of F/F 290_1 of the 1st step becomes high-level, switch SW23a and SW23b which are provided in the 1 output D/I converter 230d in the RGB D/I converter 220c in which this F/F 290_1 is formed will become one. If switch SW23a and SW23b become one, since between the gate drain short-circuits, TFTT22 for current memory / output of the 1 output D/I converter 230d will operate in a saturation region. Then, if it will be in a stable state, according to the current capability of TFTT22, the gate voltage will be set up so that the reference current from a reference current source may flow between the drain sauce of TFTT22.

[0144]After being in a stable state, signal municipal solid waste_1 is set to a low level, and. If output signal municipal solid waste_2 of F/F of the 2nd step becomes high-level, switch SW23a and SW23b which are the 1 output D/I converters 230d in the RGB D/I converter 220c in which F/F 290_1 was formed will be come by off. At this time, the voltage that TFTT22 sends reference current is held by the capacitative element C2 which is the 1 output D/I converter 230d in the RGB D/I converter 220c in which F/F 290_1 was formed. Since the end of the capacitative element C2 is connected to the gate for [TFTT20 and T21] an output, the objects TFTT20 thru/or T22 for an output can send the current corresponding to eyes, the current corresponding to eyes 2 gradation, and the current corresponding to eyes 4 gradation 1 gradation corresponding to each current capability ratio. Such a signal municipal solid waste makes a high-level period 3 output-current storage duration in the RGBD/I converter 220c. On the other hand, switch SW23a and SW23b in the RGB D/I converter 220c in which F/F of the 2nd step was provided become one, and in the state where it was stabilized. It operates in a saturation region so that reference current may flow between the drain sauce of TFTT22, and according to the current capability of TFTT22, gate voltage is set up so that the reference current may flow.

[0145]In current storage duration, the above 3 output-current storage duration is repeated about all the RGB D/I converters 220c, and reference current is memorized by all the 1 output D/I converters 230d.

[0146]In the current driving period (the 1st operation period), the vertical scanning circuit 300 chooses the control line of one line at a time.

[0147]If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1 output D/I converter 230d for every output synchronizing with this. If the digital gradation data D0 thru/or D2 is inputted, according to these levels (the high level (H) / low level (L)), ON and OFF of the switches SW20 thru/or SW22 will be controlled, The current memorized in the current driving period of the last frame is outputted according to the current capability of every TFTT20 thru/or T22. As a result, gray scale representation as shown in Table 1 becomes possible. Therefore, an output current value can be adjusted with the digital gradation data inputted from 0 to 7xi0. Since the reference current corresponding to eyes is memorized according to TFTT2 current-capability dispersion 4 gradation by current storage duration (the 2nd operation period) and the current corresponding to eyes is outputted 4 gradation in TFTT22, the current of accuracy high as current corresponding to eyes 4 gradation can be outputted. Although the current outputted in TFTT20 and T21 is eyes and a thing corresponding to eyes 2 gradation 1 gradation, respectively, these current values are below half of the current of eyes 4 gradation, and even if it changes a current value with current capability dispersion, if it compares with the case where eyes vary 4 gradation, it is small [the influence]. Therefore, even when

some current dispersion is in a proximity region, high-precision current can be supplied.
[0148]On the other hand, in a current driving period (the 1st operation period), the shift register does not operate but all the switch SW23a and SW23b are still OFF always.
[0149]And by repeating the above operations about each frame, in the indicator 400, the display according to the gradation data D0 thru/or D2 is performed, and highly precise current is supplied to a pixel circuit in that case.
[0150]According to such 14th example, since reference current is 4 times the minimum value of the reference current in the 1st example, the charge and discharge of the load of the wiring which sends reference current can be performed at high speed, and it can be quickly made a stable state. Therefore, since current storage duration can be shortened and a current driving period can be lengthened, it is possible to secure charge and discharge time, such as load which wiring to the pixel in an indicator has, for a long time. For this reason, the current of still higher accuracy can be supplied to a pixel.
[0151]Like the 2nd thru/or the 10th example to the 14th example, In composition as a pixel circuit shows drawing 38 (b), the polarity of a transistor may be changed, A transistor may be used as a switch and output current accuracy may be raised by adding shifting mutually the timing of OFF of switch SW23a and SW23b, and a transistor. Only TFTT22 does not use current as the transistor memorized and outputted, but it memorizes and is made to output current also for TFTT21, and even when a proximity region differs in increasing reference current further, the current of higher accuracy can be supplied. For example, in the semiconductor device for light-emitting displays of the 13th or 14th example, it becomes possible about the 1-bit D/I conversion circuit of the example of the 1st thru/or 12 to raise 1 or the accuracy for two or more bits by 1 or adding more than one at the 1 output D/I conversion circuit of the example of the 13th or 14.
[0152]Next, the 15th example of this invention is described. The 15th example is applied to the pixel circuit shown, for example in drawing 38 (a). Drawing 22 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 15th example of this invention.
[0153]The D/I converter 210d is formed in the 15th example, and to this D/I converter 210d. The shift register which comprised n flip-flop (F/F) 290c_1 thru/or 290 c_n which were provided every 1 output D/I converters 230e for the number of outputs to a light-emitting display (3xn) and three outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, the inversion signal ICLB of this clock signal ICL, and current selector-signals ISEL1 are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230e, and either the reference current IR0 thru/or IR2 for referring to it, IG0 to IG2, IB0 to IB2 are inputted into it according to the luminescent color assigned to it. Reference current is the current value whose luminescent color suited to red and the current-luminance property of each blue and green light emitting device, current value irof reference current IR00 -- the luminescent color -- a red light emitting device -- corresponding to eyes 1 gradation -- current value irof reference current IR11 -- the luminescent color -- a red light emitting device -- corresponding to eyes 2 gradation -- current value irof reference current IR22 -- the luminescent color -- red -- it corresponds to eyes 4 gradation. the same -- 1 gradation whose luminescent color of the current value of the reference current IG0 thru/or IG2 is green respectively -- eyes and 2 gradation -- eyes -- corresponding to eyes 4 gradation -- 1 gradation of blue [reference current / IB0 thru/or IB2 / luminescent color] respectively -- eyes and 2 gradation -- eyes -- it corresponds to eyes 4 gradation. The current selector signals ISEL1 and ISEL2 are inputted into the 1 output D/I converter 230e. The one RGB D/I converter 220d comprises the three 1 output D/I converters 230e into which the signals MSWA and MSWB outputted from one F/F 290c and this F/F 290c are inputted.
[0154]Drawing 23 is a block diagram showing the composition of the 1 output D/I converter 230e. The output blocks 240a and 240b and the data creation circuit 232 where the 1 output D/I converter 230e is constituted by the three 1-bit D/I converters 231, respectively are provided. It is controlled by the current selector signals ISEL1 and ISEL2, respectively, and switch SW31

which chooses from which block whether current is outputted among the output blocks 240a and 240b, and SW32 are provided. The data creation circuit 232 generates the data signal D0A thru/or D2A and D0B thru/or D2B based on the digital gradation data D0 thru/or D2 and the current selector signals ISEL1 and ISEL2 for one output. The data signal D0A thru/or D2A are inputted into the output block 240a, and the data signal D0B thru/or D2B are inputted into the output block 240-2. The output signal MSWA of F/F 290c is inputted into the output block 240a, and the output signal MSWB of F/F 290c is inputted into the output block 240b. The reference current I0 thru/or I2 for referring to it is inputted into the output blocks 240a and 240b. Since the 1-bit D/I converter 231 has the same composition as the thing of the 1st example and the current-luminance property of a light emitting device has proportionality, the relation between ir1=2xir0 and ir2=4xir0 is realized. Similarly it is the 1-bit D/I converter 231 provided in the object for the green (G) display, or the 1 output D/I converter 230 for a blue (B) display, Reference current IG0 or IB0, reference current IG1 or IB1, reference current IG2, or IB2 are inputted into that into which the gradation data D0, D1, and D2 are inputted, respectively.

[0155]Drawing 24 is a circuit diagram showing the composition of an example of the data creation circuit 232. NAND gate NAND0A thru/or NAND2A which considers current selector-signals ISEL1 as one input in the data creation circuit 232, for example, Inverter IV0A which reverses these outputs, respectively thru/or IV2A, NAND gate NAND0B which considers current selector-signals ISEL2 as one input or NAND2B, inverter IV0B which reverses these outputs, respectively, or IV2B is provided. The gradation data D0 is further inputted into NAND gate NAND0A and NAND0B, the gradation data D1 is further inputted into NAND gate NAND1A and NAND1B, and the gradation data D2 is further inputted into NAND gate NAND2A and NAND2B. And the data signal D0A thru/or D2A and D0B thru/or D2B are outputted, respectively from inverter IV0A thru/or IV2A and IV0B thru/or IV2B. However, this composition is an example, and if it can output the same signal, it is very good in other composition.

[0156]Next, operation of the semiconductor device for light-emitting displays concerning the 15th example constituted as mentioned above is explained. Drawing 25 is a timing chart which shows operation of the semiconductor device for light-emitting displays concerning the 15th example of this invention.

[0157]Since it begins to carry out the vertical scanning of the indicator 400 (refer to drawing 35), the period until the next vertical scanning starts is made into one frame. In the case of this example, two kinds of frames to which one side of the exclusive current selector signals ISEL1 and ISEL2 becomes high-level mutually appear by turns.

[0158]First, the 1st frame is explained. In current selector-signals ISEL1, in the 1st frame, high level and current selector-signals ISEL2 become a low level. In this case, in the output blocks 240a and 240b, by the 1st output block 240a into which the digital image data DA0 thru/or DA2 is inputted, and current is outputted. [switch SW1] On the other hand, in the 2nd output block 240b into which digital-image-data DB0 thru/or DB2 are inputted, switch SW2 turns off and current is memorized. In details, the 1-bit D/I converter 231 in the output block 240b memorizes any one of the reference current IR0 thru/or IR2, IG0 to IG2, IB0 to the IB2 more. However, in this frame, digital-gradation-data DB0 thru/or DB2 are in a low level, and switch SW1 of the 1-bit D/I converter 231 in the output block 240b has become OFF.

[0159]Next, the operation which memorizes the current of the output block 240b is explained.

[0160]With the start of the 1st frame, a pulse signal is inputted into F/F290c_1 of the 1st step as the start signal IST, Simultaneously with the input of this pulse signal, the shift register which comprises n F/F290 begins to operate in the clock signal ICL and the clock inversion signal ICLB being inputted into F/F290c_1. If output signal MSWB_of F/F290c_1 of 1st step 1 becomes high-level, the switches SW2 and SW3 of the 1-bit each D/I converter 231 of the output block 240b provided in the 1 output D/I converter 230e into which this output signal MSWB_1 is inputted will serve as one. If the switches SW2 and SW3 are turned on, since between the gate drain short-circuits, TFTT1 for current memory / output in the 1-bit D/I converter 231 will operate in a saturation region. And where this operation is stabilized, according to the current capability of TFTT1, the gate voltage is set up so that reference current may flow between the drain sauce of TFTT1.

[0161]After being in a stable state, signal MSWB_1 is set to a low level, and. If output signal MSWB_2 of F/F of the 2nd step becomes high-level, the switches SW2 and SW3 in the output block 240b provided in the 1 output D/I converter 230e in the RGB D/I converter 220d in which F/F 290_1 was formed will serve as OFF. At this time, the gate voltage of TFTT1 of the output block 240b in the RGB D/I converter 220d in which F/F 290_1 was formed is held at the voltage that reference current flows by the capacitative element C1. As a result, it is not concerned with each current capability, but reference current is memorized by TFTT1. Such a signal municipal solid waste makes a high-level period 3 output-current storage duration in the RGB D/I converter 220d. On the other hand, the switches SW2 and SW3 of the output block 240b in the RGB D/I converter 220d in which F/F of the 2nd step was provided serve as one, and in the state where it was stabilized. It operates in a saturation region so that reference current may flow between the drain sauce of TFTT1 of the 1-bit D/I converter 231, and according to the current capability of TFTT1, gate voltage is set up so that the reference current may flow.
[0162]In the 1st frame period, the above 3 output-current storage duration is repeated about the 2nd output block 240b in all the RGBD/I converters 220d, and reference current is memorized by the 2nd output block 240b of all the 1 output D/I converters 230e.
[0163]Next, operation of the 1st output block 240a in the 1st frame is explained. With the 1st frame, the vertical scanning circuit 300 chooses the control line of one line at a time. The scanning pulse Y_1 which is the 1st line and 2nd-line output, and Y_2 are shown in drawing 25.
[0164]If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1st output block 240a in the 1 output D/I converter 230e for every output synchronizing with this. If the digital gradation data D0 thru/or D2 is inputted, according to these levels (the high level (H) / low level (L)), ON and OFF of switch SW1 in the 1-bit D/I converter 231 will be controlled, The current memorized by TFTT1 in the current driving period of the last frame is outputted, and gray scale representation is performed.
[0165]As shown in Table 1, an output current value can be adjusted with the digital gradation data inputted from 0 to 7xi0. Since gate voltage is set up so that current equivalent to a reference current source may flow according to the current capability of TFTT1 with the last frame, and it is outputting using the TFTT1 [same], regardless of current capability dispersion, dispersion in output current is small and high accuracy is obtained.
[0166]On the other hand, in the 1st frame, the output MSWA of a shift register is always a low level, and the switches SW2 and SW3 in all the output blocks 240a are still OFF always.
[0167]In the 2nd following frame, operation of the 1st output block 240a and operation of the 2nd output block 240b are replaced by making high-level a low level and current selector-signals ISEL2 for current selector-signals ISEL1. As a result, the 1st output block 240a memorizes current, and the 2nd output block 240b outputs current.
[0168]By repeating the above operation every two frames, this example can supply highly precise current to a pixel circuit. In this example, since two output blocks are provided in one output, in each frame, since current is outputted, one output block is used, and the output block of another side can be used in order to memorize current, and does not independently need to provide current storage duration. Thereby, all 1 frame periods turn into a current driving period, and it becomes possible to secure charge and discharge time, such as load which wiring to the pixel in an indicator has, for a long time. Therefore, the current of still higher accuracy can be supplied to a pixel.
[0169]To the 15th example, the 2nd thru/or the 14th example may be applied and the same effect can be acquired.
[0170]The cycle of current memory will not be limited for every frame, and may be every several frames.Since the period of current memory becomes long by carrying out the cycle of current memory every several frames, current can be memorized in still higher accuracy. However, it is needed for the gate voltage corresponding to the current at the time of memory for the change below the accuracy called for by leak of a transistor, etc. not to arise.
[0171]Next, the 16th example of this invention is described. The 16th example establishes a precharge circuit in the latter part of a 1 output D/I converter. Drawing 26 is a block diagram

showing the composition of the semiconductor device for light-emitting displays concerning the 16th example of this invention.

[0172]The D/I converter 210e is formed in the 16th example. The D/I converter 210e has the same composition as the D/I converter 210d in the 16th example except for the point that the precharge circuit 250 is established in the latter part of the one output each D/I converter 230e, respectively. A precharge signal PC input is carried out in the precharge circuit 250.

[0173]the period when the precharge circuit 250 is set up by a precharge signal -- each output **** of the D/I converter 210d -- the voltage decided by the output current of the 1 output D/I converter is outputted instead of the output current of the 1 output D/I converter 230e. Drawing 27 is a circuit diagram showing the example of composition of the precharge circuit 250. The N channel transistors T31 thru/or T33 and the P channel transistor T34 which are controlled by precharge signal PC are provided in the precharge circuit 250. The output current IOUT from the 1 output D/I converter 230e is inputted into one end of the transistors T31 and T32, and the non-inversed input terminal of the dummy load circuit 252 and the operational amplifier 251 is connected to the other end of the transistor T31. In the false addition circuit 252, one end of the transistor T33 is connected to the transistor T31, and the gate of the P channel transistor T35 is connected to the other end of the transistor T33. The voltage VEL is supplied to the sauce of the transistor T35, and the other end is connected to the transistor T31. The output signal of operational amplifier 251 the very thing is inputted into the inversed input terminal of the operational amplifier 251, one end of the transistor T32 is connected to the output terminal of the operational amplifier 251, and the other end is connected to the other end of the transistor T34. The driving current of a light emitting device is outputted from the common node of the transistors T32 and T34.

[0174]In such a precharge circuit 250, it is determined whether for the output current IOUT of the 1 output D/I converter 230e to be made into the output current Iout, and to carry out a direct output with the transistor T34, or output to the dummy load circuit 252. It is determined by the transistor T32 whether the output of the operational amplifier 251 is considered as the output of the D/I converter 210e. Since the operational amplifier 251 is carrying out negative feedback of the output to the inversion input, it carries out the voltage follower output of the voltage inputted into a noninverting input. The transistor T35 is the same transistor as TFTT102 of the pixel circuit (drawing 38 (a)) in the indicator 400, or a transistor which has equivalent current capability. However, it is good also as composition which short-circuits between the gate drains of the transistor T35, and does not form the transistor T33 as the dummy load circuit 252. The transistor T31, T32, and T34, If it has composition which can also consider it as a reverse polar transistor, and inputs the precharge signal PC itself and its inversion signal, for example with some polarity of precharge signal PC in order to act as a switch, it is also possible to use what kind of polar transistor.

[0175]Next, operation of the precharge circuit 250 is explained. Drawing 28 is a timing chart which shows operation of the precharge circuit 250.

[0176]In this example, an one-line selection period is divided into the 1st period and 2nd period by the level of precharge signal PC.

[0177]In the 1st period, precharge signal PC has become high-level, and it is a precharge period. If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1 output D/I converter 230e for every output synchronizing with this. The 1 output D/I converter 230e outputs current according to the relation shown in Table 1 from the inputted digital gradation data DA0 thru/or DA2. If precharge signal PC serves as a high bell at this time, the transistor T34 in the precharge circuit 250 will serve as OFF, and the transistors T31 and T32 will serve as one. Therefore, in the precharge circuit 250, the output current of the 1 output D/I converter 230e flows into the dummy load circuit 252. Since the transistor T35 is formed in the dummy load circuit 252, when the output current Iout is stabilized and it flows, the gate voltage of the transistor T35 turns into gate voltage when the output current Iout stabilized and flows into the pixel circuit in an indicator, and the almost same voltage. And this voltage serves as an input of the voltage follower constituted by the operational amplifier 252, and in this

precharge period, since the transistor T32 serves as one, the output of a voltage follower turns into an output of the D/I converter 210e. Therefore, in this period, the gate voltage of the transistor T35 can be impressed to the pixel circuit in an indicator.

[0178]Since the dummy load circuit 252 has the wiring load very smaller than a pixel circuit etc. which need to be and carry out charge and discharge near the 1 output D/I converter 230e, At very high speed, operation of stabilizing and sending the fixed output current of the 1 output D/I converter 230e through the transistor T35 can be performed, even when an output current value is low as compared with the case where the pixel circuit in an indicator is driven by the fixed output current of a 1 output D/I conversion circuit. Since operation of impressing the gate voltage of the transistor T35 to the pixel circuit in an indicator is also performed with the output of low impedance called a voltage follower, it is realizable at high speed.

[0179]Precharge signal PC serves as a low level, and the 2nd period is a current output period. When precharge signal PC serves as a low level, the transistor T34 in the precharge circuit 250 serves as one, and the transistors T31 and T32 serve as OFF. Therefore, in the precharge circuit 250, the output current of the 1 output D/I converter 230e is outputted as it is, and the pixel circuit in an indicator drives. Since precharge operation is performed in the 1st period at this time, when the output current of the 1 output D/I converter 230e is stabilized and it flows, near voltage is impressed to the pixel circuit in an indicator. Therefore, in the 2nd period, operation of amending current capability dispersion between transistor TFTT102 (drawing 38 (a)) in the pixel circuit in the transistor T35 and an indicator, and operation of it being stabilized in the pixel circuit in an indicator, and driving the output current Iout to it are performed. As a result, the quantity which carries out the charge and discharge of the wiring load etc. in the 2nd period is small, and ends. Therefore, the 2nd period can shorten a period compared with the case where precharge operation is not performed. After outputting stable voltage by precharge operation, it can operate without being influenced by the state in front of an one-line selection period in order to perform a current drive.

[0180]Then, in the scanning pulse Y_1, a low level and the scanning pulse Y_2 become high-level, the control line of the 2nd line is chosen, and the same operation is repeated. By the above operation, the pixel circuit in an indicator can be driven at high speed by the current of still higher accuracy.

[0181]The same effect can be acquired even if it applies, when the circuit and the semiconductor device which may apply the 1st thru/or the 15th example as a 1 output D/I converter of the 16th example, and supplies current are not contained in this invention.

[0182]Next, the 17th example is described. The 17th example changes the composition of the precharge circuit in the 16th example. Drawing 29 is a block diagram showing the composition of the precharge circuit in the 17th example of this invention.

[0183]In addition to the component of the precharge circuit 250, the N channel transistor T36 and the P channel transistors T37 and T38 into which precharge signal PC is inputted are provided in the precharge circuit 250a in the 17th example. The transistor T38 is connected between the output terminal of the operational amplifier 251, and the inversed input terminal. The capacitative element C3 is inputted into the output terminal of the operational amplifier 251, the transistor T36 is connected between the other end and inversed input terminal, and the transistor T37 is connected between non-inversed input terminals.

[0184]The precharge circuit 250a constituted in this way, By having a circuit which cancels the offset voltage of the operational amplifier 251 known well, and performing offset cancellation operation at a current driving period, it cannot be influenced by the offset voltage of the operational amplifier 251, but precharge operation can be performed. Other operations are the same as operation of the precharge circuit 250 in the 16th example.

[0185]Next, the 18th example of this invention is shown in drawing 32. The data register 203 in which the 18th example holds the digital data signal inputted, The shifting-data register 202 which outputs the scanning signal which synchronized with the timing to hold, It is the horizontal drive circuit 200 provided with the data latch 204 which holds the signal of all the data registers synchronizing with a latch signal, and is outputted to the D/I converter 210, and the D/I converter 210 which outputs current according to a digital data signal. The D/I converter 210

may also include a precharge circuit. The D/I converter 210 may comprise a D/I converter of the example of either [this invention] the 1st thru/or the 17th either.
[0186]Next, the 19th example of this invention is shown in drawing 33. The 19th example can increase the data line and the pixel circuit which can be driven without the output of the D/I converter 210 of the 18th example being having enabled it to connect with the data line of two or more indicators 400 one by one, and increasing circuit structure by the selector circuit 211.
[0187]Next, the 20th example of this invention is shown in drawing 34. The 20th example builds the reference current source 212 which creates reference current in the 18th example in the horizontal drive circuit 200.
[0188]In the 1st of this invention thru/or the example of 20, although TFT explains the transistor, it may comprise a more general transistor and two or more horizontal drive circuits 200 may be used to one indicator. The indicator 400, the horizontal drive circuit 200, and the vertical scanning circuit 300 may be formed on the same substrate by creating all the transistors by TFT. In this case, highly precise precharge is realizable by creating the load of the indicator 400, and the load (circuit) of the same composition for the load (circuit) of the precharge circuit in the example of this invention.
[0189]Although the 1st of this invention thru/or the example of 20 explain the example driven by 4096 color specification as which 0 gradation - the triplet digital gradation data of 7 gradation displays input the light-emitting display provided with the light emitting device whose current-luminance property is proportionality in the color (R, G, B), respectively, A monochromatic case or the more nearly same composition also in the case of a multi-bit is extensible as it is. Although all transistors are set to TFT, this invention is realizable by same composition also with a more general transistor. Although drawing 38 (a) is assumed as a pixel circuit of an active matrix system, this invention is [as opposed to / other pixels of a simple matrix system or pixel circuits of a current drive system / again] realizable by same composition.
[0190]The above examples are applied also to a current load device provided with a more general current load device, although it is explaining in a light-emitting display provided with a light-emitting display device.
[0191]
[Effect of the Invention]As explained in full detail above, according to this invention, highly precise current can be supplied to the cell (circuit) of a current load device. This by memorizing the voltage between gate sauce in the state where reference current flows stably between the drain sauce of the transistor in digital one / current conversion device, It is for outputting current with the transistor which could memorize high-precision current and also memorized current, without receiving influence in current capability dispersion of a transistor. According to current capability dispersion in a proximity region, the number of the transistors which memorize and output current can also be fluctuated. When there is little current to memorize and the current value is large, time to memorize can be shortened and the time for charge and discharge can secure the data line in a current load device, and the load of a pixel for a long time by extending time (it drives) to output. Therefore, the cell (circuit) of a much more highly precise current load device can be supplied. The transistor for current memory and the transistor for current outputs can be provided for every output terminal, and time (it drives) to stop needing storage duration separately and output by replacing it for every frame, can be extended. As a result, highly precise current can be supplied to the cell (circuit) of a current load device.
[0192]By having the precharge circuit provided with the dummy load circuit between the output of digital one / current conversion device, and the current load device, even when an output current value is low, the pixel (circuit) of current or a device can be driven at high speed. In the initial stage of an output, this by the current output of digital one / current conversion device. Drive a dummy load circuit at high speed, and the voltage obtained from a dummy load circuit is supplied to the cell (circuit) in a current load device in a voltage follower, Voltage when the current output of digital one / current conversion device is mostly impressed to the cell (circuit) in a current load device can be impressed at high speed, Then, it is because the amount of charges and discharges of the pixel in the current load device by constant current or the load of a signal wire can be reduced by performing operation of driving and amending the cell (circuit) in

a current load device in the current output of digital one / current conversion device directly.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention]This invention about the current load device provided with the semiconductor device for a current load device drive for driving a current load device provided with two or more cells having contained the current load device, and it, It is related with the current load device provided with the semiconductor device for a current load device drive and it which perform a gradation display with the current value to which especially a current load device is supplied.

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PRIOR ART

[Description of the Prior Art]it is current load device **** as which operation is determined by the current supplied -- the current load device which equips matrix form with two or more cells is developed. The application is a light-emitting display whose current load device is a light emitting device, for example.
It is the organic electroluminescence display in which the organic EL device is used as a light emitting device.

[0003]Hereafter, taking the case of a light-emitting display, it explains as a current load device. Drawing 35 shows the composition of a matrix type light-emitting display.
[0004]A display comprises the horizontal drive circuit 200, the vertical-scanning (drive) circuit 300, and the indicator 400. A gradation display is realized by adjusting the current which flows into the light emitting device in the one pixel display part 100 of the indicator 400. In the light emitting device as which luminosity is determined by various current, current and luminosity are in proportionality. The drive method of a light-emitting display is classified into simple matrix driving and an active-matrix drive according to combination with the current or voltage impressed from the composition, the horizontal drive circuit 200, and the vertical scanning circuit 300 of the one pixel display part 100.
[0005]Drawing 36 is a circuit diagram showing the composition of one pixel display part in the case of simple matrix driving. In the one pixel display part 101 in the case of simple matrix driving, the light emitting device 130 is connected between the control line 110 and the signal wire 120 on each intersection of the control line 110 and the signal wire 120. As shown in drawing 35, the control line 110 is driven by the vertical scanning circuit 300, and drives the signal wire 120 by the horizontal drive circuit 200.
[0006]And if current or voltage is outputted to the Lth signal wire 120 from the horizontal drive circuit 200 in the period which the control line 110 is chosen one by one by the vertical scanning circuit 300 for [every], and is scanning the Kth control line 110, The current which flows into the Kth line light emitting device of the Lth row is determined, and the light emitting device emits light by the intensity corresponding to the current. Then, if the scan of eye ** (K+1) watch is started, luminescence of the light emitting device of the Kth line will be ended.
[0007]Drawing 37 is a circuit diagram showing the composition of one pixel display part in an active-matrix drive. In the one pixel display part 102 in an active-matrix drive. On each intersection of the control line 110 and the signal wire 120, switch SW100 controlled by potential of the control line 110 is connected to the signal wire 110, The gate of TFT(Thin Film Transistor: thin film transistor) T100 and one end of the capacitative element C100 are connected to the other end of switch SW100. The sauce of TFTT100 and the other end of the capacitative element C100 are grounded, and the light emitting device 130 is connected for the drain and potential of TFTT100 between the signal wires of VEL.
[0008]And if the control line 110 is chosen one by one by the vertical scanning circuit 300 for [every] and the Kth control line 110 is chosen, switch SW100 in the one pixel display part 102 will become one. At this time, the Lth output voltage of the horizontal drive circuit 200 turns into gate voltage of TFTT100, and the impedance of TFTT100 will be determined if the gate voltage

that TFTT100 operates in a saturation region is impressed. As a result, the current which flows into the light emitting device 130 is determined, and the light emitting device 130 emits light by the intensity corresponding to that current.

[0009]In an active-matrix drive, one pixel display part may take other composition. Drawing 38 (a) and drawing 38 (b) are the circuit diagrams showing other composition of one pixel display part in an active-matrix drive. As shown in drawing 38 (a), in the one pixel display part 103 of other composition, switch SW102 controlled by potential of the control line 110 is connected to the signal wire 110, and the gate and drain of P channel TFTT102 are connected to the other end of switch SW102. Switch SW101 controlled by potential of the control line 110 is connected to this gate and drain, and the gate of P channel TFTT101 and one end of the capacitative element C100 are connected to that other end. The constant potential VEL is supplied to the sauce of TFTT101 and T102, and the other end of the capacitative element C100. The light emitting device 130 is connected between the drain of TFTT101, and earth-potentials GND.

[0010]And if the Kth control line 110 is chosen by the vertical scanning circuit 300 and the switches SW101 and SW102 serve as one, the gate voltage of TFTT102 will be decided so that the Lth output current of the horizontal drive circuit 200 may be sent from the signal wire 120. Since TFTT102 and TFTT101 have taken current mirror composition, when the current capability of TFTT102 and TFTT101 is mutually equal, It lets TFTT101 pass, the same current as the output current value of the horizontal drive circuit 200 flows into the light emitting device 130, and the light emitting device 130 emits light by the intensity according to the current value.

[0011]Same operation is performed also when N channels TFTT103 and T104 are used instead of P channels TFTT101 and T102, as shown in drawing 38 (b).

[0012]Since voltage is accumulated in the capacitative element also after the following line is chosen in an active-matrix drive if simple matrix driving is compared with an active-matrix drive, sending current can be continued. Therefore, compared with the case of the simple matrix driving of only emitting light momentarily, the current sent through a light emitting device becomes small.

[0013]Thus, even if the absolute values of current or voltage differ, in not being concerned with the kind of drive method of simple matrix driving and an active-matrix drive but performing a gradation display, the horizontal drive circuit 200 has the function to change digital gradation data into current or voltage. However, since dispersion in dispersion of the threshold of a transistor, the voltage-current characteristic of a light emitting device, and current-luminance property exists that it is a voltage output in a pixel circuit (one pixel display part), even if it impresses the same voltage, a possibility that luminosity varies is high. On the other hand, since it is influenced only by dispersion in the current-luminance property of a light emitting device in the case of a current output, the small and high-precision display of dispersion in luminosity is attained.

[0014]Drawing 39 is a block diagram showing an example of the composition of the horizontal drive circuit 200 for outputting current to the indicator 400. In this composition, after developing digital gradation data by the data logic section 201 in several output minutes, the current output for several output minutes is obtained in inputting those digital gradation data into digital one / current conversion part 210.

[0015]Drawing 40 is a circuit diagram showing the 1st conventional example of digital one / current conversion part for one output. When gradation data is a triplet (D0 thru/or D2), common connection of switch SW110 controlled by these, respectively, SW111, and SW112 is carried out to the outgoing end which outputs the current Idata. N channelTFTT110 and T111 by which input voltage VA is supplied to a gate, respectively, and T112 are connected between switch SW110, SW111, SW112, and the earthing conductor in the earth potentials VG. The current-luminance property of a light emitting device shall be in proportionality. The case where both the horizontal drive circuit 200 and the vertical scanning circuit 300 are formed on a glass substrate is assumed, and all transistors serve as TFT. Even when gradation data is more than a triplet, it is constituted similarly.

[0016]In the 1st conventional example, it is designed so that each channel length (L) may become fixed and the ratio of channel width (W) may be set to 1:2:4 about TFTT110, T111, and

T112. In TFTT110 thru/or T112, since gate voltage serves as voltage VA and source voltage is all common with the voltage VG, when TFTT110 thru/or TT112 are operating in the saturation region, a current ratio is set to 1:2:4. Therefore, if suitable input voltage VA is chosen, the current output of 8 gradation used as 0-7 of a current ratio will become possible about the output current Idata by turning on and off the switches SW110 thru/or SW112 based on the gradation data D0 thru/or D2. The absolute value of current can be adjusted by changing input voltage VA.

[0017]Drawing 41 is a circuit diagram showing the 2nd conventional example of digital ones / current conversion part for one output. In the 2nd conventional example, the digital gradation data D0 thru/or D2 is inputted into the gate of N channels TFTT110 thru/or T112. Common connection of the drain of TFTT110 thru/or T112 is carried out to an outgoing end, and the power supply voltage VD is supplied to sauce. The ratio of the channel width of TFTT110 thru/or T112 is set as 1:2:4 like the 1st conventional example.

[0018]By considering it as the level which sets the high level of the digital-gradation-data input as suitable voltage beforehand and with which a thin film transistor turns off a low level in such 2nd conventional example instead of forming a switch. The current output of 8 gradation used as 0-7 of a current ratio becomes possible like the 1st conventional example. The absolute value of current can be adjusted by changing the high level of a digital-gradation-data input.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention]As explained in full detail above, according to this invention, highly precise current can be supplied to the cell (circuit) of a current load device. This by memorizing the voltage between gate sauce in the state where reference current flows stably between the drain sauce of the transistor in digital one / current conversion device, It is for outputting current with the transistor which could memorize high-precision current and also memorized current, without receiving influence in current capability dispersion of a transistor. According to current capability dispersion in a proximity region, the number of the transistors which memorize and output current can also be fluctuated. When there is little current to memorize and the current value is large, time to memorize can be shortened and the time for charge and discharge can secure the data line in a current load device, and the load of a pixel for a long time by extending time (it drives) to output. Therefore, the cell (circuit) of a much more highly precise current load device can be supplied. The transistor for current memory and the transistor for current outputs can be provided for every output terminal, and time (it drives) to stop needing storage duration separately and output by replacing it for every frame, can be extended. As a result, highly precise current can be supplied to the cell (circuit) of a current load device.
[0192]By having the precharge circuit provided with the dummy load circuit between the output of digital one / current conversion device, and the current load device, even when an output current value is low, the pixel (circuit) of current or a device can be driven at high speed. In the initial stage of an output, this by the current output of digital one / current conversion device. Drive a dummy load circuit at high speed, and the voltage obtained from a dummy load circuit is supplied to the cell (circuit) in a current load device in a voltage follower, Voltage when the current output of digital one / current conversion device is mostly impressed to the cell (circuit) in a current load device can be impressed at high speed, Then, it is because the amount of charges and discharges of the pixel in the current load device by constant current or the load of a signal wire can be reduced by performing operation of driving and amending the cell (circuit) in a current load device in the current output of digital one / current conversion device directly.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, in a transistor, especially TFT, since dispersion in current capability when the same gate voltage is impressed between different TFT (s) is large, there is a problem that it is difficult to take out a high-precision current output. In the conventional digital one / current conversion part, if there is characteristic dispersion of TFT throughout current load device width mostly, even if the size of TFT is uniform and the voltage between gate sauce is uniform, since a current value differs from other fields, display unevenness will occur in the scattered portion. If the characteristic of TFT which will be used for the output same in display unevenness occurring between adjacent pixels if current capability varies and the dispersion becomes large also between TFT(s) which are in a proximity region varies, it stops also satisfying the monotonicity of gradation.
[0020]In especially the conventional digital one / current conversion part, in an active-matrix drive, when an output current value is low, there is also a problem that a drive takes time. If the active-matrix drive by current drive is adopted, when the same current as the output current of digital one / current conversion part which is a drive circuit flows into TFT in a pixel, a drive will complete this, but. It is because it is necessary to carry out the charge and discharge of those volume loads by the output current which is constant current since wiring load, especially parasitic capacitance certainly exist in the signal wire 110 in the indicator 400 and a light emitting device also has capacity value in it. That is, since the same current as the output current of digital one/current conversion circuit which is a drive circuit flows into TFT in a pixel only after carrying out the charge and discharge of those capacity to a certain voltage, it takes long time by then.
[0021]This invention was made in view of this problem, and is ****. The purpose can supply high-precision output current to **** digital image data, It is providing the light-emitting display provided with the semiconductor device for a light-emitting display drive and it which can drive a light-emitting display at high speed, even when [desirable] an output current value's is low, and providing the current load device provided with still more general semiconductor device for a current load device drive and it.

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MEANS

[Means for Solving the Problem]A semiconductor device for a current load device drive concerning this invention, In a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device, A function to memorize a current value of n (n is natural number) kind determined by one sort or two or more sorts of reference current inputted, It has at least one n bit digital / current conversion circuit provided with a function which outputs one current according to n bit digital data inputted among current values of 2^n level obtained from said memory current value for every supply terminal to said one or more cells.
[0023]Other semiconductor devices for a current load device drive concerning this invention, In a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device, have two or more current output circuits and a precharge circuit, and said precharge circuit, It is characterized by it being possible to supply voltage it is decided by output current of said current output circuit that will be a cell on said data line via the data line in said current load device, and to supply output current of said current output circuit as it is.
[0024]Furthermore it starts this invention, others a semiconductor device for a current load device drive, In a semiconductor device for a drive of a current load device provided with two or more cells having contained a current load device, Two or more n bit digital / current conversion circuits which memorize one or more reference current values, and output current according to n bit digital data, A shift register for current memory which outputs a scanning signal which synchronizes with storage operation of said reference current of said n bit digital / current conversion circuit performed one by one, n bit data latch which transmits n bit digital data to n bit-data selector, and said n bit digital / current conversion circuit by whether operation which memorizes said reference current is performed, or operation which outputs current is performed. It has at least n bit-data selector which decides whether to transmit n bit digital data from said n bit data latch to n bit digital / current conversion circuit.
[0025]And the composition is as follows when this invention is applied to a semiconductor device for a light-emitting display drive, or a light-emitting display.
[0026]Namely, the 1st semiconductor device for a light-emitting display drive concerning this invention, In a semiconductor device for a light-emitting display drive with which a light emitting device it is decided with current supplied that luminosity will be drives a light-emitting display provided in each pixel, A reference current value for 1 bit. n 1-bit digital / current conversion circuits to memorize. To 1, or two or more 1-bit digital / current conversion circuits which each preparation inputted reference current of n kind corresponding to the current-luminance property of said light emitting device memorized in said one 1-bit digital / current conversion circuit, and were chosen based on digital image data of n bit, said reference current. It is set as what has n bit digital / current conversion circuit which outputs current of 2^n kind for every output terminal which outputs current to said light-emitting display, and doubled it one by one to a current value with the respectively lowest current value of said n kind of reference current by making it output.
[0027]Said 1-bit digital / current conversion circuit, A signal wire in which said reference current

flows, and the data line with which 1 bit of said digital image data is transmitted, The control line, the 1st and 2nd voltage supply lines, and the 1st transistor by which sauce was connected to said 1st voltage supply line, A capacitative element connected between a gate of said 1st transistor, and said 2nd voltage supply line, The 1st switch controlled by a signal which is connected between a drain of said 1st transistor, and said output terminal, and transmits said data line, The 2nd switch controlled by a signal which is connected between drains of a gate of said 1st transistor, said signal wire, or said 1st transistor, and transmits said control line, The 3rd switch controlled by a signal which is connected between a drain of said 1st transistor, and said signal wire, and transmits said control line, A signal wire in which it may **** and said reference current flows, the data line with which 1 bit of said digital image data is transmitted, the 1st and 2nd control lines, the 1st and 2nd voltage supply lines, and the 1st transistor by which sauce was connected to said 1st voltage supply line, A capacitative element connected between a gate of said 1st transistor, and said 2nd voltage supply line, The 1st switch controlled by a signal which is connected between a drain of said 1st transistor, and said output terminal, and transmits said data line, The 2nd switch controlled by a signal which is connected between drains of a gate of said 1st transistor, said signal wire, or said 1st transistor, and transmits said 2nd control line, It may have the 3rd switch controlled by a signal which is connected between a drain of said 1st transistor, and said signal wire, and transmits said 1st control line.

[0028]Or a gate may have the 2nd transistor by which bias was carried out between said 1st transistor and said 1st voltage supply line.

[0029]When said 2nd and 3rd switches are ON states in an OFF state, said 1st switch said transistor, Voltage between gate sauce of said transistor in a stage which between the gate drain connected too hastily, operated in a saturation region, and was stabilized in the operation, If it becomes voltage required in order to send said reference current between drain sauce, and the value will be determined according to current capability of said transistor and the 2nd and 3rd switches of an account of back to front will be in an OFF state, If it is determined by operation of said 1st switch whether voltage between gate sauce of said transistor is held at said capacitative element, and reference current based on voltage between this held gate sauce is outputted, Since each output has said n 1-bit digital / current conversion circuits, according to said n bit digital image data, current of 2^n level according to the current-luminance property of said light emitting device can be outputted. Therefore, said 1-bit digital / current conversion circuit cannot be concerned with current capability dispersion of a transistor which memorizes and outputs said current, but can output current of high accuracy.

[0030]Since influence of a noise by OFF operation of a transistor as said 3rd switch will become small if said 3rd switch is turned off after said 2nd switch is turned off, Said 1-bit digital / current conversion circuit can memorize and output current more at high degree of accuracy.

[0031]Said 1st [the] thru/or the 3rd switch may comprise a transistor.

[0032]To said 1-bit digital / current conversion circuit. Said 2nd control line. Dummy transistors which were 1/2 of a product of the length of a gate of a transistor and width from which an inversion signal of a signal to transmit is inputted into a gate, and a product of the length of a gate and width constitutes said 2nd switch, and a drain was connected to a gate of said transistor and sauce connected with a drain too hastily. Since movement of an electric charge at the time of a transistor as said 2nd switch turning off by providing can be compensated, as for said 1-bit digital / current conversion circuit, current can be memorized and outputted more at high degree of accuracy.

[0033]In this invention, in current storage duration, the 1st transistor that memorizes n current in n bit each digital / current conversion circuit short-circuits between gate drains, it is operating in a saturation region, and voltage between gate sauce is the voltage into which reference current stabilizes and flows. At the time of an end of current storage duration, a switch which has short-circuited between gate drains is turned off, and voltage between said gate sauce is saved in capacity. It is holding voltage between gate sauce which is not concerned with current capability dispersion of said 1st n transistor, but sends reference current in order to memorize voltage between gate sauce through which said 1st n transistor sends reference

current according to each current capability at this time, and current is memorized. In a driving period, the 1st transistor that memorized said n current, It decides whether output memorized current by turning on and off n switches between each drain of the 1st transistor that memorized said n current, and an output of said digital one/current conversion circuit according to image digital data. Since current outputted in this way is outputted from the transistor itself which memorized said n current, it becomes a thing without influence of current capability dispersion which has high accuracy. By the above operations, n bit digital / current conversion circuit of this invention become possible [outputting current with high accuracy from which a current ratio becomes 0, 1, 2, ..., 2^{n-1}]. In this case, in order to constitute n bit digital / current conversion circuit, n reference current sources are needed.

[0034]When said gate has the 2nd transistor by which bias was carried out, Cascode connection is made, and said 1st transistor and the 2nd transistor can stop dispersion in current supplied, even if the characteristic of a light emitting device varies, since the drain voltage dependency of drain current can be suppressed when operating in both saturation regions.

[0035]The 2nd semiconductor device for a light-emitting display drive concerning this invention, In a semiconductor device for a light-emitting display drive with which a light emitting device it is decided with current supplied that luminosity will be drives a light-emitting display provided in each pixel, Memorize one sort of reference current values, and current of 2^{n} kind corresponding to the current-luminance property of said light emitting device is generated from said memorized reference current based on digital image data of n bit. It has n bit digital / current conversion circuit to output for every output terminal which outputs current to said light-emitting display.

[0036]Said n bit digital / current conversion circuit, A signal wire in which said reference current flows, and the data line of n book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The control line, the 1st and 2nd voltage supply lines, and a transistor for current memory by which sauce was connected to said 1st voltage supply line, n transistors for current outputs which a gate short-circuits mutually and by which common connection of the sauce was carried out to the 1st voltage supply line, A capacitative element connected between a gate of said transistor for current outputs, and said 2nd voltage supply line, n switches for output controls controlled by either of the signals which is connected between a drain of said n transistors for current outputs, and said output terminal, respectively, and transmits said data line, The 1st switch for storage controls controlled by a signal which is connected between a drain of said transistor for current memory, and said signal wire, and transmits said control line, The 2nd switch for storage controls controlled by a signal which is connected between a gate of said transistor for current memory, and a gate of said transistor for current outputs, and transmits said control line, It **** and current capability of said n transistors for current outputs may be set as what was doubled one by one to the respectively lowest current capability, A signal wire in which said reference current flows through n bit digital / current conversion circuit, The data line of n book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The 1st and 2nd control lines, the 1st and 2nd voltage supply lines, and a transistor for current memory by which sauce was connected to said 1st voltage supply line, n transistors for current outputs which a gate short-circuits mutually and by which common connection of the sauce was carried out to the 1st voltage supply line, A capacitative element connected between a gate of said transistor for current outputs, and said 2nd voltage supply line, n switches for output controls controlled by either of the signals which is connected between a drain of said n transistors for current outputs, and said output terminal, respectively, and transmits said data line, The 1st switch for storage controls controlled by a signal which is connected between a drain of said transistor for current memory, and said signal wire, and transmits said 2nd control line, Have the 2nd switch for storage controls controlled by a signal which is connected between a gate of said transistor for current memory, and a gate of said transistor for current outputs, and transmits said 1st control line, and current capability of said n transistors for current outputs, It may be set as what was doubled one by one to the respectively lowest current capability.

[0037]Or a gate may have the bias transistor by which bias was carried out, respectively

between said transistor for current memory, said transistor for current outputs, and said 1st voltage supply line.

[0038]When the said 1st and 2nd switches for storage controls are ON states in the state of OFF of said switch for output controls, said transistor for current memory, Voltage between gate sauce of said transistor for current memory in a stage which between the gate drain connected too hastily, operated in a saturation region, and was stabilized in the operation, If it becomes voltage required in order to send said reference current between drain sauce, and the value is determined according to current capability of said transistor for current memory and the account 1st of back to front and the 2nd switch for storage controls are turned off, Voltage between gate sauce of said transistor for current memory is held at said capacitative element, Said n transistors for current outputs will be in the state where current of n kind can be sent with the total based on each current capability from reference current based on voltage between this held gate sauce, It may be determined by digital image data whether whose current which said transistor for current outputs can send is outputted it is said n bit.

[0039]As for said 2nd switch for storage controls, it is preferred to be turned off, after said 1st switch for storage controls is turned off.

[0040]The said switch for output controls, 1st, and 2nd switches for storage controls may comprise a transistor.

[0041]Said n bit digital / current conversion circuit, Said 2nd control line. An inversion signal of a signal to transmit. Dummy transistors which were 1/2 of a product of the length of a gate of a transistor and width from which it is inputted into a gate and a product of the length of a gate and width constitutes said 1st switch for storage controls, and a drain was connected to a gate of said transistor for current memory, and sauce connected with a drain too hastily. Having is preferred.

[0042]This invention can be used when current capability dispersion of a transistor in a proximity region is small. A transistor which memorizes current in said n bit digital / current conversion circuit memorizes current by the same means as the 1st semiconductor device concerning above-mentioned this invention. They are a transistor which memorizes said current, a transistor which outputs said current, and current mirror composition here, A current capability ratio is 1:2:4. : ... Current capability most a current capability ratio with a large transistor among n transistors for an output which are :2 $^{n-1}$ like 1:1 or 2:1, If a transistor which memorizes current is made equally or large, a reference current value becomes large, and since a period which carries out the charge and discharge of the wiring load in which reference current flows is shortened, current storage duration can be shortened. Since a transistor which memorizes said current at this time memorizes gate source voltage in the state where reference current flowed, it is not based on dispersion in current capability, but can memorize current in high accuracy. Therefore, when current capability dispersion of a transistor in a proximity region is small, By having as a means, n switches switch on and off according to digital input image data between a drain of said transistor for an output, and an output of said n bit digital / current conversion circuit. A current ratio becomes possible [outputting current with high accuracy used as 0, 1, 2, ..., 2^{n-1}]. n bit digital / current conversion circuit can be constituted from one reference current source in this case, and a required input can be lessened.

[0043]When said gate has here the bias transistor by which bias was carried out, Said transistor for current memory, said transistor for current outputs, and said bias transistor, Cascode connection is made, and since the drain voltage dependency of drain current can be suppressed when operating in both saturation regions, even if the characteristic of a light emitting device varies, dispersion in current supplied can be stopped.

[0044]The 3rd semiconductor device for a light-emitting display drive concerning this invention, In a semiconductor device for a light-emitting display drive with which a light emitting device it is decided with current supplied that luminosity will be drives a light-emitting display provided in each pixel, Reference current of k kind corresponding to the current-luminance property of said light emitting device. Memorize and current of a seed from said memorized k kind of reference current (n-k). It has n bit digital / current conversion circuit which generates and outputs

current of a 2^n kind based on digital image data of n bit from combination of these current for every output terminal which outputs current to said light-emitting display.

[0045]Said n bit digital / current conversion circuit, A signal wire of k book with which said reference current flows, and the data line of n book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The control line, the 1st and 2nd voltage supply lines, and k transistors for a current memory output by which sauce was connected to said 1st voltage supply line, A transistor for current outputs of an individual (n-k) which a gate connected with any one of said k transistors for a current memory output too hastily, 1 or two or more capacitative elements which were connected between a gate of said transistor for a current memory output, and said 2nd voltage supply line, n switches for output controls controlled by either of the signals which is connected between a drain of said transistor for a current memory output, and said transistor for current outputs, and an output terminal, respectively, and transmits said data line, The 1st k switch for storage controls controlled by a signal which is connected between a drain of said transistor for a current memory output, and said signal wire, and transmits said control line, Have the 2nd k switch for storage controls controlled by a signal which is connected between a gate of said transistor for a current memory output, and a drain, and transmits said control line, and current capability of each of said transistor for current outputs, Rather than that of said all transistors for a current memory output, it is low and current capability of said transistor for current outputs, and said transistor for a current memory output, It may be set as what was doubled one by one to the respectively lowest current capability, and said n bit digital / current conversion circuit, A signal wire of k book with which said reference current flows, and the data line of n book with which it is alike, respectively and 1 bit of said digital image data is transmitted, The 1st and 2nd control lines, the 1st and 2nd voltage supply lines, and k transistors for a current memory output by which sauce was connected to said 1st voltage supply line, A transistor for current outputs of an individual (n-k) which a gate connected with any one of said k transistors for a current memory output too hastily, 1 or two or more capacitative elements which were connected between a gate of said transistor for a current memory output, and said 2nd voltage supply line, n switches for output controls controlled by either of the signals which is connected between a drain of said transistor for a current memory output, and said transistor for current outputs, and an output terminal, respectively, and transmits said data line, The 1st k switch for storage controls controlled by a signal which is connected between a drain of said transistor for a current memory output, and said signal wire, and transmits said 2nd control line, The 2nd k switch for storage controls controlled by a signal which is connected between a gate of said transistor for a current memory output, and a drain, and transmits said 1st control line, It ****, and current capability of each of said transistor for current outputs is lower than that of said all transistors for a current memory output, and current capability of said transistor for current outputs and said transistor for a current memory output may be set as what was doubled one by one to the respectively lowest current capability.

[0046]Or a gate may have the bias transistor by which bias was carried out, respectively between said transistor for current memory, said transistor for current outputs, and said 1st voltage supply line.

[0047]When said switch for output controls is [the said 1st and 2nd switches for storage controls] ON states in an OFF state, said transistor for a current memory output, Voltage between gate sauce of said transistor for a current memory output in a stage which between the gate drain connected too hastily, operated in a saturation region, and was stabilized in the operation, If it becomes voltage required in order to send said reference current between drain sauce, and the value is determined according to current capability of said current and a transistor for a memory output and the account 1st of back to front and the 2nd switch for storage controls are turned off, Voltage between gate sauce of said transistor for a current memory output is held at said capacitative element, A transistor for said transistor for current outputs, current memory, and an output will be in the state where current of n kind can be sent with the total based on each current capability from reference current based on voltage between

this held gate sauce, It may be determined by digital image data whether whose current which said transistor for current outputs and a transistor for a current memory output can send is outputted it is said n bit.
[0048]As for said 2nd switch for storage controls, it is preferred to be turned off, after said 1st switch for storage controls is turned off.
[0049]The said switch for output controls, 1st, and 2nd switches for storage controls may comprise a transistor.
[0050]Said n bit digital / current conversion circuit, Said 2nd control line. An inversion signal of a signal to transmit. Dummy transistors which were 1/2 of a product of the length of a gate of a transistor and width from which it is inputted into a gate and a product of the length of a gate and width constitutes said 1st switch for storage controls, and a drain was connected to a gate of said current memory and a transistor for an output, and sauce connected with a drain too hastily. Having is preferred.
[0051]This invention can be used when current capability dispersion of a transistor in a proximity region is a little small. In current storage duration, 1 in n bit digital / current conversion circuit means thru/or said some of current memory, and a transistor for an output memorize reference current of a transistor and the same number by the same means as ****. Therefore, 1 which memorizes said current – some transistors can output current of high accuracy. On the other hand, a transistor which memorizes and outputs said current, and 1 which is current mirror composition – some transistors for an output are making it output current lower than said reference current, and even when current capability varies, they can make influence in the whole small. By the above composition, a current ratio is 1:2:4. : ... Current which is :2^{n-1} can be supplied in high accuracy, By having as a means, n switches which turn on and off said current according to digital input image data between a drain of a transistor memorized and outputted or said transistor for an output, and an output of said digital one/current conversion circuit. A current ratio becomes possible [outputting current with high accuracy used as 0, 1, 2, ..., 2^{n-1}]. Digital one/current conversion circuit can be constituted from 1 thru/or some reference current sources in this case, and an input from the outside can be lessened.
[0052]When said gate has here the bias transistor by which bias was carried out, Said transistor for current memory, said transistor for current outputs, and said bias transistor, Cascode connection is made, and since the drain voltage dependency of drain current can be suppressed when operating in both saturation regions, even if the characteristic of a light emitting device varies, dispersion in current supplied can be stopped.
[0053]This invention can constitute n bit digital / current conversion circuit means combining digital one / current conversion circuit means of above-mentioned either of the 1st to 3. By for example, a thing for which bit (n-1) digital / current conversion circuit of the 2nd invention in a bit not more than it are used for a bit with the highest current value using said 1-bit digital / current conversion circuit of the 1st invention. While accuracy of a large bit with the highest current value of influence of dispersion is high, reference current can constitute n bit digital / current conversion circuit whose number is two.
[0054]In this invention, said 1st and 2nd voltage supply lines may be used as a common power source wire.
[0055]When the luminescent color whose number of said output terminals is a pixel of a and said light-emitting display is a b color, nx b sorts of reference current values are needed again, but. Because digital one/current conversion circuit which current storage operation may be performed in an a/b step, and is equivalent to one output at this time have said two n bit digital / current conversion circuits. In arbitrary frames, it is more preferred that make one side into a circuit for current outputs, make another side into a circuit for current memory, memory of current is performed in an a/b step using the same reference current within each frame, and a role of a current output and current memory is replaced for every frame. By replacing a frame rate for every frame, a period for memorizing current other than a period which drives a light-emitting display is not needed. Therefore, a period to drive can be considered to be the whole frame period, and can take one long horizontal period which drives one line, and it becomes

possible to drive highly precise current to a pixel circuit. Above-mentioned operation is the same even when digital one/current conversion circuit equivalent to said one output are provided with said three or more n bit digital / current conversion circuits for example. Every multiple frame may replace a role of a current output and current memory.

[0056]This invention has a precharge circuit which outputs suitable voltage in current outputted from a current output circuit like said n bit digital / current conversion circuit being inputted, A dummy load circuit which said precharge circuit will serve as load equivalent to said light emitting device if said light-emitting display is a simple matrix type, and will serve as load equivalent to a pixel circuit if said light-emitting display is an active matrix system, A voltage follower which considers voltage when output current from said current output circuit flows into said dummy load circuit as an input, The 1st switch for precharge connected between an output of said current output circuit, and said dummy load circuit, The 1st control line for precharge that transmits a signal which controls said 1st switch for precharge, The 2nd switch for precharge that connects an output and said light-emitting display of said current output circuit, The 2nd control line for precharge that transmits an inversion signal of a signal which controls said 2nd switch for precharge and controls said 1st switch for precharge, It is preferred to have the 3rd switch controlled by a signal which is connected between an output of said voltage follower and said light-emitting display, and transmits said 1st control line for precharge.

[0057]Output current of said current output circuit is supplied to said dummy load circuit as precharge operation in early stages of one horizontal period, The voltage is impressed to a light emitting device or said pixel circuit in said pixel in said light-emitting display via a voltage follower, By supplying output current of said current output circuit to a light emitting device or said pixel circuit in said pixel in said light-emitting display directly as the aftercurrent drive operation, Since time for charge and discharge can shorten wiring load in said light-emitting display, etc. even when output current of said current output circuit is small, a light emitting device or said pixel circuit in said pixel in said light-emitting display can be driven more to stability and a high speed, and high degree of accuracy.

[0058]By providing again composition which cancels offset voltage of said voltage follower in said precharge circuit, By performing operation which cancels offset voltage of said voltage follower at the time of said current drive operation. Since a difference at the time of supplying a pixel (circuit) in a case where output current of a circuit which excessive time is unnecessary, and also memorizes and outputs said current is supplied to said dummy load circuit, and said actual light-emitting display becomes small, A light emitting device or said pixel circuit in said pixel in said light-emitting display can be driven more to stability and a high speed, and high degree of accuracy.

[0059]Since said false pixel (circuit) is near said the digital one/current conversion circuit by providing a precharge circuit, even when wiring load in the meantime is small and current outputted is small, said false pixel (circuit) comes to send outputted current stably in short time. Input into a voltage follower gate voltage in the state where current is flowing into said false pixel (circuit) stably, and an output of said voltage follower by connecting with the data line of a light-emitting display. Voltage with output current of said current output circuit near voltage in the state where it is flowing into a pixel (circuit) in said indicator stably is impressed to a pixel (circuit) in said signal wire or said indicator. The above precharge operation can perform load of said data line at high speed compared with carrying out charge and discharge by constant current. After voltage of a pixel (circuit) in said data line and said indicator is stabilized by precharge operation, said false pixel (circuit) is separated from said current output circuit, and current is outputted to said data line directly from said current output circuit. In this case, charge and discharge of load of said data line by constant current which is an output of said current output circuit, or a pixel (circuit) in said indicator, Since precharge has already been performed, what is necessary is just to carry out slightly, and it is not influenced by load of said signal wire before precharge, voltage of a pixel (circuit) in said indicator, etc. Driving time can be shortened. Therefore, it becomes possible stability and to carry out the current drive of the pixel (circuit) at high speed and with high precision, without being influenced by performing two steps of above drive operation by voltage of wiring load of light-emitting display circles before a drive,

or load of a pixel (circuit).
[0060]A semiconductor device for a light-emitting display drive concerning this invention, For every output, memorize reference current and said n bit digital / current conversion circuit which outputs current of 2^n kind according to n bit digital data One or more preparations, And by whether said n bit digital / current conversion circuit perform an output or storage operation of current. It has a data selector which performs whether data from n bit data latch and said n bit data latch is transmitted to said n bit digital / current conversion circuit, and has a shift register for current memory which outputs a scanning signal which synchronized with operation which memorizes said reference current as the whole device further. Said semiconductor device for a light-emitting display drive has said precharge circuit for every output again. Said semiconductor device for a light-emitting display drive is provided with n bit data register which holds n bit digital data which is inputted from the outside, and which is inputted synchronizing with a scanning signal of a shift register for data-hold for every output, and is provided with said shift register for data-hold as the whole device. By what it has further an output selector circuit connectable [in one horizontal period / an output of said n bit digital / current circuit, or said precharge circuit] with two or more data lines of a light-emitting display one by one according to selector signals for. Said semiconductor device for a light-emitting display drive can drive a light-emitting display by less circuit structure.
[0061]One chip may be accumulated with a circuit which generates said reference current. A transistor may comprise a thin film transistor.
[0062]It has one which was accumulated by one chip with a circuit which a light-emitting display concerning this invention is formed in the same substrate as said light emitting device, and generates said reference current of the above-mentioned semiconductor devices for a light-emitting display drive.
[0063]When said light emitting device and a semiconductor device for a light-emitting display drive are especially formed in the same substrate, since dummy load (circuit) in said precharge circuit can be constituted from same size as load (circuit) in a pixel of a display, and shape, it can make accuracy of precharge voltage obtained high. At this time, the driving method which combined above-mentioned precharge operation and current output operation can be driven more to stability, a high speed, and high degree of accuracy.
[0064]A semiconductor device for a light-emitting display drive and a light-emitting display of this invention are applicable also to a semiconductor device and a current load device for driving a more common current load device and a current load device which comprise a current load device instead of as above-mentioned. [a light emitting device]
[0065]
[Embodiment of the Invention]The semiconductor device for light-emitting displays is taken for an example like ****, and the semiconductor device for current load devices concerning the example of this invention is concretely explained with reference to an attached drawing. In attaching and showing an underbar and a number when an order is set up by the same component, and observing separately, it shows the following explanation, without attaching an underbar and a number.
[0066]Drawing 1 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 1st example of this invention. Digital one / current (D/I) converter 210 is formed in the 1st example, The shift register which comprised the n flip-flops (F/F) 290_1 thru/or 290_n provided in this D/I converter 210 every 1 output D/I converters 230 for the number of outputs to a light-emitting display (3xn) and three outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, and the inversion signal ICLB of this clock signal ICL are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230, and either the reference current IR0 thru/or IR2 for referring to it, IG0 to IG2, IB0 to IB2 are inputted into it according to the luminescent color assigned to it. Reference current is the current value whose luminescent color suited to red and the current-luminance property of each blue and green light emitting device, current value irof reference current IR00 -- the luminescent color -- a red light

emitting device -- corresponding to eyes 1 gradation -- current value irof reference current IR11 -- the luminescent color -- a red light emitting device -- corresponding to eyes 2 gradation -- current value irof reference current IR22 -- the luminescent color -- red -- it corresponds to eyes 4 gradation. the same -- 1 gradation whose luminescent color of the current value of the reference current IG0 thru/or IG2 is green respectively -- eyes and 2 gradation -- eyes -- corresponding to eyes 4 gradation -- 1 gradation of blue [reference current / IB0 thru/or IB2 / luminescent color] respectively -- eyes and 2 gradation -- eyes -- it corresponds to eyes 4 gradation. The one RGB D/I converter 220 comprises the three 1 output D/I converters 230 into which signal municipal solid waste outputted from one F/F290 and this F/F290 is inputted.

[0067]Drawing 2 is a block diagram showing the composition of the 1 output D/I converter 230. The 1 output D/I converter 230 comprises the three 1-bit D/I converters 231. In these 1-bit D/I converters 231, respectively The image data D0 and the combination of the reference current I0, Either of the combination of the combination of the image data D1 and the reference current I1, the image data D2, and the reference current I2 is inputted, and signal municipal solid waste which is an output signal of F/F is inputted. The reference current I0 thru/or I2 corresponds to the combination of the reference current IR0 thru/or IR2, the combination of the reference current IG0 thru/or IG2, or combination of the reference current IB0 thru/or IB2. That is, in the 1 output D/I converter 230 for a red (R) display, the reference current supplied to the 1-bit D/I converter 231 into which the digital gradation data D0 is inputted is reference current IR0 corresponding to the luminosity of eyes 1 gradation of the light emitting device for red displays. The reference current supplied to the 1-bit D/I converter 231 into which the digital gradation data D1 is inputted, It is reference current IR1 corresponding to the luminosity of eyes 2 gradation of the light emitting device for red displays, and the reference current supplied to the 1-bit D/I converter 231 into which the digital gradation data D2 is inputted is reference current IR2 corresponding to the luminosity of eyes 4 gradation of the light emitting device for red displays. However, since the current-luminance property of a light emitting device has proportionality, the relation between ir1=2xir0 and ir2=4xir0 is realized. Similarly it is the 1-bit D/I converter 231 provided in the object for the green (G) display, or the 1 output D/I converter 230 for a blue (B) display, Reference current IG0 or IB0, reference current IG1 or IB1, reference current IG2, or IB2 are inputted into that into which the gradation data D0, D1, and D2 are inputted, respectively.

[0068]Drawing 3 is a block diagram showing the composition of the 1-bit D/I converter 231. The transistor N channel thin film transistor (TFT) T1, the switches SW1 thru/or SW3, and the capacitative element C1 for current memory / output are provided in the 1-bit D/I converter 231. It is connected to the drain of TFTT1 and switch SW1 is controlled by gradation data D*. The output current Iout is outputted from the other end of switch SW1. It is connected between the point of contact with the switches SW1 and TFTT1, and the end of the capacitative element C1 and the gate of TFTT1, and switch SW2 is controlled by signal municipal solid waste. One end of switch SW3 is connected to the signal wire in which reference current I* is supplied, it is connected between the point of contact with the switches SW1 and TFTT1, and one end of the capacitative element C1, and the other end is controlled by signal municipal solid waste. Although the sauce of TFTT1 and the other end of the capacitative element C1 are grounded, for example, when there is no operation top problem, voltage higher than ground voltage GND may be supplied.Gradation data D* and reference current I* are equivalent to either the gradation data D0 and the reference current I0, the gradation data D1 and the reference current I1, the gradation data D2 and the reference current I2.

[0069]Next, operation of the semiconductor device for light-emitting displays concerning the 1st example constituted as mentioned above is explained. Drawing 4 is a timing chart which shows operation of the semiconductor device for light-emitting displays concerning the 1st example of this invention. Y_1 in drawing 4, and Y_2, respectively The 1st line of the vertical scanning circuit 300 (refer to drawing 35), The output signal of the 2nd line is shown and D0, D1, and D2 show triplet digital image data (gradation data), Iout shows the output signal of the 1 output D/I converter 230, and IST shows the start signal of the shift register which comprises the n flip-

flops 290, ICL shows the clock signal of a shift register and municipal solid waste_1 and municipal solid waste_2 show the output signal of the 1st step of a shift register, and the 2nd step, respectively.

[0070]Since it begins to carry out the vertical scanning of the indicator 400 (refer to drawing 35), the period until the next vertical scanning starts is made into one frame. One frame comprises a current driving period (the 1st operation period) and current storage duration (the 2nd operation period).

[0071]First, current storage duration (the 2nd operation period) is explained. In current storage duration, the 1-bit each D/I converter 231 memorizes the reference current supplied to each from the reference current source. Here, in this period, all the digital gradation data is made into a low level, and switch SW1 of the 1-bit D/I converter 231 is off.

[0072]With the start of current storage duration, a pulse signal is inputted into F/F 290_1 of the 1st step as the start signal IST, Simultaneously with the input of this pulse signal, the shift register which comprises n F/F290 begins to operate in the clock signal ICL and the clock inversion signal ICLB being inputted into F/F 290_1. If output signal municipal solid waste_1 of F/F 290_1 of the 1st step becomes high-level, the switches SW2 and SW3 of the 1-bit each D/I converter 231 provided in the 1 output D/I converter 230 into which this output signal municipal solid waste_1 is inputted will serve as one. If the switches SW2 and SW3 are turned on, since between the gate drain short-circuits, TFTT1 for current memory / output in the 1-bit D/I converter 231 will operate in a saturation region. And where this operation is stabilized, according to the current capability of TFTT1, the gate voltage is set up so that the reference current from a reference current source may flow between the drain sauce of TFTT1.

[0073]If signal municipal solid waste_1 is set to a low level and output signal municipal solid waste_2 of F/F of the 2nd step becomes high-level after being in a stable state, the switches SW2 and SW3 of the 1-bit each D/I converter 231 in the RGB D/I converter 220 in which F/F 290_1 was formed will be come by off. At this time, the gate voltage of TFTT1 in the RGBD/I converter 220 in which F/F 290_1 was formed is held at the voltage that reference current flows by the capacitative element C1. As a result, it is not concerned with each current capability, but reference current is memorized by TFTT1. Such a signal municipal solid waste makes a high-level period 3 output-current storage duration in the RGB D/I converter 220. On the other hand, each switches SW2 and SW3 in the RGB D/I converter 220 in which F/F of the 2nd step was provided serve as one, and in the state where it was stabilized. It operates in a saturation region so that reference current may flow between the drain sauce of TFTT1, and according to the current capability of TFTT1, gate voltage is set up so that the reference current may flow.

[0074]In current storage duration, the above 3 output-current storage duration is repeated about all the RGB D/I converters 220, and reference current is memorized by all the 1 output D/I converters 230.

[0075]Next, a current driving period (the 1st operation period) is explained. In the current driving period, the vertical scanning circuit 300 chooses the control line (scanning line) of one line at a time. The scanning pulse Y_1 which is the 1st line and 2nd-line output, and Y_2 are shown in drawing 4.

[0076]If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1 output D/I converter 230 for every output synchronizing with this. If the digital gradation data D0 thru/or D2 is inputted, according to these levels (the high level (H) / low level (L)), ON and OFF of switch SW1 in the 1-bit D/I converter 231 will be controlled, and the current memorized by TFTT1 in the current driving period of the last frame will be outputted. The relation between the input digital gradation data D0 thru/or D2 and gradation (output current value) is shown in the following table 1.

[0077]

[Table 1]

階調	階調データ			出力電流値 (Ｉｏｕｔの電流値)
	Ｄ０	Ｄ１	Ｄ２	
０	Ｌ	Ｌ	Ｌ	０
１	Ｈ	Ｌ	Ｌ	ｉ０
２	Ｌ	Ｈ	Ｌ	ｉ１＝２×ｉ０
３	Ｈ	Ｈ	Ｌ	ｉ１＋ｉ０＝３×ｉ０
４	Ｌ	Ｌ	Ｈ	ｉ２＝４×ｉ０
５	Ｈ	Ｌ	Ｈ	ｉ２＋ｉ０＝５×ｉ０
６	Ｌ	Ｈ	Ｈ	ｉ２＋ｉ１＝６×ｉ０
７	Ｈ	Ｈ	Ｈ	ｉ２＋ｉ１＋ｉ０＝７×ｉ０

[0078]As shown in Table 1, an output current value can be adjusted with the digital gradation data inputted from 0 to 7xi0. Since gate voltage is set up so that current equivalent to a reference current source may flow according to the current capability of TFTT1 by current storage duration (the 2nd operation period), and current is outputted using the TFTT1 [same], Regardless of dispersion in current capability, dispersion in output current is small and high accuracy is obtained.
[0079]On the other hand, in a current driving period (the 1st operation period), the shift register does not operate but all the switches SW2 and SW3 are still OFF always.
[0080]And by repeating the above operations about each frame, in the indicator 400, the display according to the gradation data D0 thru/or D2 is performed, and highly precise current is supplied to a pixel circuit in that case.
[0081]According to such 1st example, current can be supplied in a high speed and high accuracy to the light-emitting display which has P channel TFT as shown in drawing 38 (a).
[0082]Next, the 2nd example of this invention is described. The 2nd example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (b). Drawing 5 is a block diagram showing the composition of the 1-bit D/I converter in the 2nd example of this invention.
[0083]Instead of N channel TFTT1 in the 1st example, P channel TFTT2 is provided in the 1-bit D/I converter 231a in the 2nd example, and the power supply potential VD is supplied to the end of the sauce and the capacitative element C1. The voltage VD is comparable as the voltage VEL, or is low voltage, and let it be a level which does not have a problem in operation.
[0084]The 1st example can be applied when the transistor which sends the current of a pixel circuit as shown in drawing 38 (a) is P channel TFT, but the 2nd example is applicable to N channel TFT as shown in drawing 38 (b). That is, when TFT in a pixel circuit is P channel TFT, the source voltage is the voltage VEL, but when it is considered as N channel TFT, it is necessary to set the source voltage to ground level GND, and this example can respond to this.
[0085]Except for operation of the 2nd example changing the polarity of output current, it is the same as that of the 1st example, and the same effect is acquired.

[0086]Next, the 3rd example of this invention is described. The 3rd example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (a). Drawing 6 is a block diagram showing the composition of the 1-bit D/I converter in the 3rd example of this invention.
[0087]In the 1-bit D/I converter 231b in the 3rd example, not earth-potentials GND but suitable stable voltage VB is supplied to the end of the capacitative element C1.
[0088]Operation of the 3rd example is the same as that of the 1st example, and the same effect is acquired. The voltage by which this is supplied to the capacitative element C1 shows that what kind of voltage may be sufficient, if stabilized.
[0089]Next, the 4th example of this invention is described. The 4th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (b). Drawing 7 is a block diagram showing the composition of the 1-bit D/I converter in the 4th example of this invention.
[0090]In the 1-bit D/I converter 231c in the 4th example, not earth-potentials GND but suitable stable voltage VB is supplied to the end of the capacitative element C1 like the 3rd example. Like the 2nd example, P channel TFTT2 is provided instead of N channel TFTT1 in the 1st example, and the power supply potential VD is supplied to the end of the sauce and the capacitative element C1.
[0091]Thus, the 4th example is what applied the 3rd example to the 2nd example, and like the 3rd example, the voltage supplied to the capacitative element C1 shows that what kind of voltage may be sufficient, if stabilized.
[0092]Next, the 5th example of this invention is described. The 5th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (a). Drawing 8 is a block diagram showing the composition of the 1-bit D/I converter in the 5th example of this invention.
[0093]Instead of the switches SW1 thru/or SW3 in the 1st example, the N channel transistors T11 thru/or T13 are formed in the 1-bit D/I converter 231d in the 5th example, respectively.
[0094]Also by such 5th example, based on the timing chart shown in drawing 4, the same operation as the 1st example is performed, and the same effect is acquired. P channel transistor can also be used instead of the N channel transistors T11 thru/or T13. In this case, the timing chart should just reverse what shows drawing 4 the output signal of F/F.
[0095]Next, the 6th example of this invention is described. The 6th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (b). Drawing 9 is a block diagram showing the composition of the 1-bit D/I converter in the 6th example of this invention.
[0096]Instead of the switches SW1 thru/or SW3 in the 2nd example, the N channel transistors T11 thru/or T13 are formed in the 1-bit D/I converter 231e in the 6th example, respectively.
[0097]Also by such 6th example, based on the timing chart shown in drawing 4, the same operation as the 2nd example is performed, and the same effect is acquired. P channel transistor can also be used instead of the N channel transistors T11 thru/or T13. In this case, the timing chart should just reverse what shows drawing 4 the output signal of F/F.
[0098]Next, the 7th example of this invention is described. The 7th example is applied to the pixel circuit shown, for example in drawing 38 (a). Drawing 10 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 7th example of this invention.
[0099]The D/I converter 210a is formed in the 7th example, and to this D/I converter 210a. The shift register which comprised n flip-flop (F/F) 290a_1 thru/or 290 a_n which were provided every 1 output D/I converters 230a for the number of outputs to a light-emitting display (3xn) and three outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, the inversion signal ICLB of this clock signal ICL, and current memory timing signal IT are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230a, and either the reference current IR0 thru/or IR2 for referring to it, IG0 to IG2, IB0 to IB2 are inputted into it according to the luminescent color assigned to it. The one RGB D/I converter 220a comprises the three 1 output

D/I converters 230a into which the signals municipal solid waste1 and municipal solid waste2 outputted from one F/F 290a and this F/F 290a are inputted.

[0100]Drawing 11 is a block diagram showing the composition of the 1 output D/I converter 230a. The 1 output D/I converter 230a comprises the three 1-bit D/I converters 231f. In these 1-bit D/I converters 231f. Either of the combination of the combination of the combination of the image data D0 and the reference current I0, the image data D1, and the reference current I1, the image data D2, and the reference current I2 is inputted, respectively, and the signals municipal solid waste1 and municipal solid waste2 which are output signals of F/F are inputted.

[0101]Drawing 12 is a block diagram showing the composition of the 1-bit D/I converter 231f. Transistor N channelTFTT1, the N channel transistors T11 thru/or T13, and the capacitative element C1 for current memory / output are provided in the 1-bit D/I converter 231f like the 5th example. Gradation data D0 and signal municipal solid waste2 and signal municipal solid waste1 are inputted into the gate of the transistor T11, T12, and T13, respectively, and each transistor is controlled by these signals.

[0102]Next, operation of the semiconductor device for light-emitting displays concerning the 7th example constituted as mentioned above is explained. Drawing 13 is a timing chart which shows operation of the semiconductor device for light-emitting displays concerning the 7th example of this invention.

[0103]In this example, as shown in drawing 13, in current storage duration, signal municipal solid waste1 changes like signal municipal solid waste in the 1st example. Current memory timing signal IT rises synchronizing with the standup of one of signal municipal solid waste1, and falls from the signal municipal solid waste1 to early timing. And signal municipal solid waste2 rises to the same timing as signal municipal solid waste1, and it falls synchronizing with falling of current memory timing signal IT. Let the period when signal municipal solid waste2 has risen be 3 output-current storage duration in the RGB D/I converter 220a.

[0104]In such 7th example, only the transistor T12 turns off the 1-bit D/I converter 231f at the time of the end of 3 output-current storage duration, and the transistor T13 turns it off after that. Therefore, the gate voltage of TFTT1 in the state where reference current is stably sent between drain sauce is not influenced by the noise at the time of the transistor T13 turning off, but is held more correctly. For this reason, this example can supply still higher-precision current as compared with the 5th example.

[0105]Next, the 8th example of this invention is described. The 8th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 7th example, for example, is shown in drawing 38 (b). Drawing 14 is a block diagram showing the composition of the 1-bit D/I converter in the 8th example of this invention.

[0106]P channel TFTT2 is provided for N channel TFTT1 in the 7th example in the 1-bit D/I converter 231g in the 8th example instead, and the power supply potential VD is supplied to the end of the sauce and the capacitative element C1.

[0107]Except for operation of the 8th example changing the polarity of output current, it is the same as that of the 7th example, and the same effect is acquired. For example, still higher-precision current can be supplied as compared with the 6th example.

[0108]Next, the 9th example of this invention is described. The 9th example is applied to the pixel circuit shown, for example in drawing 38 (a). Drawing 15 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 9th example of this invention.

[0109]The D/I converter 210b is formed in the 9th example, and to this D/I converter 210b. The shift register which comprised n flip-flop (F/F) 290b_1 thru/or 290 b_n which were provided every 1 output D/I converters 230b for the number of outputs to a light-emitting display (3xn) and three outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, the inversion signal ICLB of this clock signal ICL, and current memory timing signal IT are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230b, and either the reference current IR0 thru/or IR2 for referring to it, IG0 to IG2, IB0 to IB2 are inputted into it according to the luminescent color assigned to it. The one RGB D/I converter 220b comprises the three 1 output

D/I converters 230b into which signal municipal solid waste1 outputted from one F/F 290b and this F/F 290b, municipal solid waste2, and municipal solid waste2B are inputted. Signal municipal solid waste2B is an inversion signal of signal municipal solid waste2.

[0110]Drawing 16 is a block diagram showing the composition of the 1 output D/I converter 230b. The 1 output D/I converter 230b comprises the three 1-bit D/I converters 231h. In these 1-bit D/I converters 231h. Either of the combination of the combination of the combination of the image data D0 and the reference current I0, the image data D1, and the reference current I1, the image data D2, and the reference current I2 is inputted, respectively, and signal municipal solid waste1 which is an output signal of F/F, municipal solid waste2, and municipal solid waste2B are inputted.

[0111]Drawing 17 is a block diagram showing the composition of the 1-bit D/I converter 231h. Transistor N channelTFTT1, the N channel transistors T11 thru/or T13, and the capacitative element C1 for current memory / output are provided in the 1-bit D/I converter 231h like the 7th example. Gradation data D0 and signal municipal solid waste2 and signal municipal solid waste1 are inputted into the gate of the transistor T11, T12, and T13, respectively, and each transistor is controlled by these signals. In this example, the N channel transistor T14 is connected between the N channel transistor T12 and the end of the capacitative element C1. The sauce and the drain of the N channel transistor 14 are short-circuited mutually, and signal municipal solid waste2B is inputted into the gate. And the gate of TFTT1 is connected to the point of contact of the drain of the N channel transistor 14, and the end of the capacitative element C1. The transistor length L of the transistor T14 and the product with the transistor width W are the halves of the transistor length L of the transistor T12, and a product with the transistor width W.

[0112]The semiconductor device for light-emitting displays concerning the 9th example constituted in this way operates like the 7th example based on the timing chart shown in drawing 13. However, the waveform of signal municipal solid waste2B reverses the waveform of signal municipal solid waste2.

[0113]Therefore, while the transistor T12 turns off the 1-bit D/I converter 231h at the time of the end of 3 output-current storage duration, and the transistor T13 turns it off later than this. [the converter] [the transistor T14] For this reason, the gate voltage of TFTT1 in the state where reference current is stably sent between drain sauce, Movement of the electric charge produced when it is not influenced by the noise at the time of the transistor T13 turning off and the transistor T12 turns off is also absorbed by one of the transistor T14, and is held much more correctly. Thus, this example can supply still higher-precision current as compared with the 7th example.

[0114]Next, the 10th example of this invention is described. The 10th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 9th example, for example, is shown in drawing 38 (b). Drawing 18 is a block diagram showing the composition of the 1-bit D/I converter in the 10th example of this invention.

[0115]P channel TFTT2 is provided for N channel TFTT1 in the 9th example in the 1-bit D/I converter 231i in the 10th example instead, and the power supply potential VD is supplied to the end of the sauce and the capacitative element C1.

[0116]Except for operation of the 10th example changing the polarity of output current, it is the same as that of the 9th example, and the same effect is acquired. For example, still higher-precision current can be supplied as compared with the 8th example.

[0117]Next, the 11th example of this invention is described. The 11th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (a). Drawing 30 is a block diagram showing the composition of the 1-bit D/I converter in the 11th example of this invention.

[0118]In the 1-bit D/I converter 231j in the 11th example, it is not connected to the point of contact of the switches SW1 and TFT1, and the gate of TFTT1, but the both ends of SW2 are connected with the signal wire in which reference current I* is supplied at the gate of TFTT1, respectively.

[0119]Operation of the 11th example is the same as that of the 1st example, and the same

effect is acquired. The 2nd to the 1st example is performed and a change like the 10th example can be made.

[0120]Next, the 12th example of this invention is described. The 12th example is applied to the pixel circuit which changes the composition of the 1-bit D/I converter in the 1st example, for example, is shown in drawing 38 (a). Drawing 31 is a block diagram showing the composition of the 1-bit D/I converter in the 12th example of this invention.

[0121]In the 1-bit D/I converter 231k in the 12th example, TFTT15 is added between TFTT1 and line GND and voltage VS1 [suitable] is impressed to the gate of TFT15.

[0122]Operation of the 12th example is the same as that of the 1st example, and the same effect is acquired. Since cascode connection of the TFTT15 and TFTT1 which were added is made, flattening of the drain voltage dependency of the drain current in the saturation region of TFT1 is carried out, and an example becomes possible [raising the accuracy of the output current Iout]. The 2nd [as opposed to the 1st example for being carried out] is performed, and this example can make a change like the 10th example.

[0123]Next, the 13th example of this invention is described. The 11th example is applied to the pixel circuit shown, for example in drawing 38 (a), and when current capability dispersion of a proximity region is small, it can be used. Drawing 19 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 13th example of this invention.

[0124]The D/I converter 210c is formed in the 13th example, and to this D/I converter 210c. The shift register which comprised the n flip-flops (F/F) 290_1 thru/or 290_n provided every the 1 output D/I converter 230c for the number of outputs to a light-emitting display (3xn) and 3 outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, and the inversion signal ICLB of this clock signal ICL are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230c, and IBreference current IR2 for referring to it, IG2, or 2 is inputted into it according to the luminescent color assigned to it. The one RGB D/I converter 220c comprises the three 1 output D/I converters 230c into which signal municipal solid waste outputted from one F/F290 and this F/F290 is inputted.

[0125]The luminescent color has doubled the current value of reference current with red and each blue and green current luminance property, current value irof reference current IR22 -- the luminescent color -- red -- it corresponds to eyes 4 gradation and current value igof reference current IG22 has the green luminescent color -- corresponding to eyes 4 gradation -- current value ibof reference current IB22 -- the luminescent color -- blue -- eyes are supported 4 gradation. That is, the reference current supplied to the 1 output D/I converter 230c for a red (R) display is reference current IR2 corresponding to the luminosity of eyes 4 gradation of the light emitting device for red displays. However, since the current-luminance property of a light emitting device has proportionality, it will be set to ir2=4xir0 if the current value corresponding to eyes is set to ir0 1 gradation. Similarly, reference current IG2 or IB2 are inputted into the object for the green (G) display, or the 1 output D/I converter 230c for a blue (B) display, respectively. Therefore, in this example, the minimum of the reference current inputted will be 4 times the 1st example. The reason for having made reference current correspond to eyes 4 gradation, It is because the current capability of N channel TFTT23 which memorizes the current provided in the 1 output D/I converter 230c like the after-mentioned, and the current capability of N channel TFTT22 which outputs the current which is equivalent to eyes 4 gradation were designed become equal.

[0126]Drawing 20 is a block diagram showing the composition of the 1 output D/I converter 230c. Switch SW23a by which it is controlled by signal municipal solid waste, and reference current I* is supplied to the end is provided in the 1 output D/I converter 230c. Common connection of the drain and gate of N channel TFTT23 is carried out to the other end of the switch 23a. The sauce of TFTT23 is grounded. One end of switch SW23b controlled by signal municipal solid waste is connected to the drain and gate of N channel TFTT23, and common connection of the gate of N channels TFTT20 thru/or T22 and the one end of the capacitative element C2 is carried out to the other end at them. The sauce of TFTT20 thru/or T22 and the

other end of the capacitative element C2 are grounded. The gradation data D0, D1, switch SW20 that are controlled by D2, SW21, and SW22 are connected to the drain of TFTT20, T21, and T22, respectively, and common connection of the other end of these switches SW20 thru/or SW22 is carried out. The output current Iout is outputted from this common node. The current capability ratio of TFTT20, T21, and T22 is 1:2:4. The current capability of TFTT22 and the current capability of TFTT23 are designed become the same mutually. When there is no operation top problem, voltage higher than earth-potentials GND instead of earth-potentials GND may be supplied to the sauce of TFTT20 thru/or T23, and the end of the capacitative element C2. For example, it may be connected to the signal wire in which only the capacitative elements C2 differ.

[0127]The semiconductor device for light-emitting displays concerning the 13th example constituted in this way operates like the 1st example based on the timing chart shown in drawing 4.

[0128]In the current storage duration (the 2nd operation period) in the 13th example, the one output each D/I converter 230c memorizes the reference current (either IR2, IG2 or IB2) supplied to each from the reference current source. Here, in this period, all the digital gradation data is made into a low level, and the switches SW20 thru/or SW22 of the 1 output D/I converter 230c are off.

[0129]With the start of current storage duration, a pulse signal is inputted into F/F 290_1 of the 1st step as the start signal IST, Simultaneously with the input of this pulse signal, the shift register which comprises n F/F290 begins to operate in the clock signal ICL and the clock inversion signal ICLB being inputted into F/F 290_1. If output signal municipal solid waste_1 of F/F 290_1 of the 1st step becomes high-level, switch SW23a and SW23b which are provided in the 1 output D/I converter 230c in the RGB D/I converter 220c in which this F/F 290_1 is formed will become one. If switch SW23a and SW23b become one, since between the gate drain short-circuits, TFTT23 for current memory of the 1 output D/I converter 230c will operate in a saturation region. Then, if it will be in a stable state, according to the current capability of TFTT23, the gate voltage will be set up so that the reference current from a reference current source may flow between the drain sauce of TFTT23.

[0130]After being in a stable state, signal municipal solid waste_1 is set to a low level, and. If output signal municipal solid waste_2 of F/F of the 2nd step becomes high-level, switch SW23a and SW23b of the 1 output D/I converter 230c in the RGB D/I converter 220c in which F/F 290_1 was formed will be come by off. At this time, the voltage that TFTT23 sends reference current is held by the capacitative element C2 of the 1 output D/I converter 230c in the RGB D/I converter 220c in which F/F 290_1 was formed. Since the end of the capacitative element C2 is connected to the gate for [TFTT20 thru/or T22] an output, the objects TFTT20 thru/or T22 for an output, Corresponding to each current capability ratio to TFTT23, the current corresponding to eyes, the current corresponding to eyes 2 gradation, and the current corresponding to eyes 4 gradation can be sent 1 gradation, respectively. Such a signal municipal solid waste makes a high-level period 3 output-current storage duration in the RGB D/I converter 220c. On the other hand, switch SW23a and SW23b in the RGB D/I converter 220c in which F/F of the 2nd step was provided become one, and in the state where it was stabilized. It operates in a saturation region so that reference current may flow between the drain sauce of TFTT23, and according to the current capability of TFTT23, gate voltage is set up so that the reference current may flow.

[0131]In current storage duration, the above 3 output-current storage duration is repeated about all the RGB D/I converters 220c, and reference current is memorized by all the 1 output D/I converters 230c.

[0132]In the current driving period (the 1st operation period), the vertical scanning circuit 300 chooses the control line of one line at a time.

[0133]If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1 output D/I converter 230c for every output synchronizing with this. If the digital gradation data D0 thru/or D2 is inputted, according to these levels (the high level (H) /

low level (L)), ON and OFF of the switches SW20 thru/or SW22 will be controlled, The current memorized in the current driving period of the last frame is outputted according to the current capability of every TFTT20 thru/or T22. As a result, gray scale representation as shown in Table 1 becomes possible. Therefore, an output current value can be adjusted with the digital gradation data inputted from 0 to 7xi0. Since reference current is memorized according to dispersion in current capability by current storage duration (the 2nd operation period) and dispersion in current capability is small in a proximity region, regardless of current capability dispersion in a big field, current dispersion is small and high accuracy is obtained.

[0134]On the other hand, in a current driving period (the 1st operation period), the shift register does not operate but all the switch SW23a and SW23b are still OFF always.

[0135]And by repeating the above operations about each frame, in the indicator 400, the display according to the gradation data D0 thru/or D2 is performed, and highly precise current is supplied to a pixel circuit in that case.

[0136]According to such 13th example, since reference current is 4 times the minimum value of the reference current in the 1st example, the charge and discharge of the load of the wiring which sends reference current can be performed at high speed, and it can be quickly made a stable state. Therefore, since current storage duration can be shortened and a current driving period can be lengthened, still higher-precision current can be supplied to the pixel in an indicator.

[0137]Like the 2nd thru/or the 12th example to the 13th example, In composition as a pixel circuit shows drawing 38 (b), the polarity of a transistor may be changed, A transistor may be used as a switch and output current accuracy may be raised by adding shifting mutually the timing of OFF of switch SW23a and SW23b, and a transistor. The minimum value of reference current can be enlarged more by making current capability of TFTT23 larger than the current capability of TFTT22, for example. In this case, since current storage duration can be shortened and a current driving period can be lengthened, charge and discharge time, such as load which wiring to the pixel in an indicator has, can be secured now for a long time, and the current of still higher accuracy can be supplied to a pixel.

[0138]Next, the 14th example of this invention is described. The 14th example is applied to the pixel circuit which changes the composition of the 1 output D/I converter in the 13th example, for example, is shown in drawing 38 (a), and when current capability dispersion of a proximity region is a little small, it can be used. Drawing 21 is a block diagram showing the composition of the 1-bit D/I converter in the 14th example of this invention.

[0139]In the 1 output D/I converter 230d in the 14th example, TFTT23 is not provided but the end of switch SW23a is connected to the drain of TFTT22. Switch SW23b is connected between the drain of TFTT22, and sauce.

[0140]Like the 13th example, the current value of reference current, the luminescent color has doubled with red and each blue and green current luminance property -- current value irof reference current IR22 -- the luminescent color -- red -- it corresponds to eyes 4 gradation and current value igof reference current IG22 has the green luminescent color -- corresponding to eyes 4 gradation -- current value ibof reference current IB22 -- the luminescent color -- blue -- eyes are supported 4 gradation. That is, the reference current supplied to the 1 output D/I converter 230d for a red (R) display is reference current IR2 corresponding to the luminosity of eyes 4 gradation of the light emitting device for red displays. However, since the current-luminance property of a light emitting device has proportionality, it will be set to ir2=4xir0 if the current value corresponding to eyes is set to ir0 1 gradation. Similarly, reference current IG2 or IB2 are inputted into the object for the green (G) display, or the 1 output D/I converter 230c for a blue (B) display, respectively. Therefore, in this example, the minimum of the reference current inputted will be 4 times the 1st example. The reason for having made reference current correspond to eyes 4 gradation is because the current capability of TFTT20 for an output of the 1 output D/I converter 230d and T21 and the current capability of TFTT22 which memorizes and outputs current were designed like the after-mentioned so that it might be set to 1:2:4.

[0141]The semiconductor device for light-emitting displays concerning the 14th example constituted in this way as well as the 1st example operates based on the timing chart shown in

drawing 4.

[0142]In the current storage duration (the 2nd operation period) in the 14th example, the one output each D/I converter 230d memorizes the reference current (either IR2, IG2 or IB2) supplied to each from the reference current source. Here, in this period, all the digital gradation data is made into a low level, and the switches SW20 thru/or SW22 of the 1 output D/I converter 230d are off.

[0143]With the start of current storage duration, a pulse signal is inputted into F/F 290_1 of the 1st step as the start signal IST, Simultaneously with the input of this pulse signal, the shift register which comprises n F/F290 begins to operate in the clock signal ICL and the clock inversion signal ICLB being inputted into F/F 290_1. If output signal municipal solid waste_1 of F/F 290_1 of the 1st step becomes high-level, switch SW23a and SW23b which are provided in the 1 output D/I converter 230d in the RGB D/I converter 220c in which this F/F 290_1 is formed will become one. If switch SW23a and SW23b become one, since between the gate drain short-circuits, TFTT22 for current memory / output of the 1 output D/I converter 230d will operate in a saturation region. Then, if it will be in a stable state, according to the current capability of TFTT22, the gate voltage will be set up so that the reference current from a reference current source may flow between the drain sauce of TFTT22.

[0144]After being in a stable state, signal municipal solid waste_1 is set to a low level, and. If output signal municipal solid waste_2 of F/F of the 2nd step becomes high-level, switch SW23a and SW23b which are the 1 output D/I converters 230d in the RGB D/I converter 220c in which F/F 290_1 was formed will be come by off. At this time, the voltage that TFTT22 sends reference current is held by the capacitative element C2 which is the 1 output D/I converter 230d in the RGB D/I converter 220c in which F/F 290_1 was formed. Since the end of the capacitative element C2 is connected to the gate for [TFTT20 and T21] an output, the objects TFTT20 thru/or T22 for an output can send the current corresponding to eyes, the current corresponding to eyes 2 gradation, and the current corresponding to eyes 4 gradation 1 gradation corresponding to each current capability ratio. Such a signal municipal solid waste makes a high-level period 3 output-current storage duration in the RGBD/I converter 220c. On the other hand, switch SW23a and SW23b in the RGB D/I converter 220c in which F/F of the 2nd step was provided become one, and in the state where it was stabilized. It operates in a saturation region so that reference current may flow between the drain sauce of TFTT22, and according to the current capability of TFTT22, gate voltage is set up so that the reference current may flow.

[0145]In current storage duration, the above 3 output-current storage duration is repeated about all the RGB D/I converters 220c, and reference current is memorized by all the 1 output D/I converters 230d.

[0146]In the current driving period (the 1st operation period), the vertical scanning circuit 300 chooses the control line of one line at a time.

[0147]If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1 output D/I converter 230d for every output synchronizing with this. If the digital gradation data D0 thru/or D2 is inputted, according to these levels (the high level (H) / low level (L)), ON and OFF of the switches SW20 thru/or SW22 will be controlled, The current memorized in the current driving period of the last frame is outputted according to the current capability of every TFTT20 thru/or T22. As a result, gray scale representation as shown in Table 1 becomes possible. Therefore, an output current value can be adjusted with the digital gradation data inputted from 0 to 7xi0. Since the reference current corresponding to eyes is memorized according to TFTT2 current-capability dispersion 4 gradation by current storage duration (the 2nd operation period) and the current corresponding to eyes is outputted 4 gradation in TFTT22, the current of accuracy high as current corresponding to eyes 4 gradation can be outputted. Although the current outputted in TFTT20 and T21 is eyes and a thing corresponding to eyes 2 gradation 1 gradation, respectively, these current values are below half of the current of eyes 4 gradation, and even if it changes a current value with current capability dispersion, if it compares with the case where eyes vary 4 gradation, it is small [the influence]. Therefore, even when

some current dispersion is in a proximity region, high-precision current can be supplied.
[0148]On the other hand, in a current driving period (the 1st operation period), the shift register does not operate but all the switch SW23a and SW23b are still OFF always.
[0149]And by repeating the above operations about each frame, in the indicator 400, the display according to the gradation data D0 thru/or D2 is performed, and highly precise current is supplied to a pixel circuit in that case.
[0150]According to such 14th example, since reference current is 4 times the minimum value of the reference current in the 1st example, the charge and discharge of the load of the wiring which sends reference current can be performed at high speed, and it can be quickly made a stable state. Therefore, since current storage duration can be shortened and a current driving period can be lengthened, it is possible to secure charge and discharge time, such as load which wiring to the pixel in an indicator has, for a long time. For this reason, the current of still higher accuracy can be supplied to a pixel.
[0151]Like the 2nd thru/or the 10th example to the 14th example, In composition as a pixel circuit shows drawing 38 (b), the polarity of a transistor may be changed, A transistor may be used as a switch and output current accuracy may be raised by adding shifting mutually the timing of OFF of switch SW23a and SW23b, and a transistor. Only TFTT22 does not use current as the transistor memorized and outputted, but it memorizes and is made to output current also for TFTT21, and even when a proximity region differs in increasing reference current further, the current of higher accuracy can be supplied. For example, in the semiconductor device for light-emitting displays of the 13th or 14th example, it becomes possible about the 1-bit D/I conversion circuit of the example of the 1st thru/or 12 to raise 1 or the accuracy for two or more bits by 1 or adding more than one at the 1 output D/I conversion circuit of the example of the 13th or 14.
[0152]Next, the 15th example of this invention is described. The 15th example is applied to the pixel circuit shown, for example in drawing 38 (a). Drawing 22 is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 15th example of this invention.
[0153]The D/I converter 210d is formed in the 15th example, and to this D/I converter 210d. The shift register which comprised n flip-flop (F/F) 290c_1 thru/or 290 c_n which were provided every 1 output D/I converters 230e for the number of outputs to a light-emitting display (3xn) and three outputs is provided. Start signal IST for the timing control which memorizes current, the clock signal ICL, the inversion signal ICLB of this clock signal ICL, and current selector-signals ISEL1 are inputted into a shift register. The digital image data D0 thru/or D2 of each output is inputted into the 1 output D/I converter 230e, and either the reference current IR0 thru/or IR2 for referring to it, IG0 to IG2, IB0 to IB2 are inputted into it according to the luminescent color assigned to it. Reference current is the current value whose luminescent color suited to red and the current-luminance property of each blue and green light emitting device, current value irof reference current IR00 -- the luminescent color -- a red light emitting device -- corresponding to eyes 1 gradation -- current value irof reference current IR11 -- the luminescent color -- a red light emitting device -- corresponding to eyes 2 gradation -- current value irof reference current IR22 -- the luminescent color -- red -- it corresponds to eyes 4 gradation. the same -- 1 gradation whose luminescent color of the current value of the reference current IG0 thru/or IG2 is green respectively -- eyes and 2 gradation -- eyes -- corresponding to eyes 4 gradation -- 1 gradation of blue [reference current / IB0 thru/or IB2 / luminescent color] respectively -- eyes and 2 gradation -- eyes -- it corresponds to eyes 4 gradation. The current selector signals ISEL1 and ISEL2 are inputted into the 1 output D/I converter 230e. The one RGB D/I converter 220d comprises the three 1 output D/I converters 230e into which the signals MSWA and MSWB outputted from one F/F 290c and this F/F 290c are inputted.
[0154]Drawing 23 is a block diagram showing the composition of the 1 output D/I converter 230e. The output blocks 240a and 240b and the data creation circuit 232 where the 1 output D/I converter 230e is constituted by the three 1-bit D/I converters 231, respectively are provided. It is controlled by the current selector signals ISEL1 and ISEL2, respectively, and switch SW31

which chooses from which block whether current is outputted among the output blocks 240a and 240b, and SW32 are provided. The data creation circuit 232 generates the data signal D0A thru/or D2A and D0B thru/or D2B based on the digital gradation data D0 thru/or D2 and the current selector signals ISEL1 and ISEL2 for one output. The data signal D0A thru/or D2A are inputted into the output block 240a, and the data signal D0B thru/or D2B are inputted into the output block 240-2. The output signal MSWA of F/F 290c is inputted into the output block 240a, and the output signal MSWB of F/F 290c is inputted into the output block 240b. The reference current I0 thru/or I2 for referring to it is inputted into the output blocks 240a and 240b. Since the 1-bit D/I converter 231 has the same composition as the thing of the 1st example and the current-luminance property of a light emitting device has proportionality, the relation between ir1=2xir0 and ir2=4xir0 is realized. Similarly it is the 1-bit D/I converter 231 provided in the object for the green (G) display, or the 1 output D/I converter 230 for a blue (B) display, Reference current IG0 or IB0, reference current IG1 or IB1, reference current IG2, or IB2 are inputted into that into which the gradation data D0, D1, and D2 are inputted, respectively.
[0155]Drawing 24 is a circuit diagram showing the composition of an example of the data creation circuit 232. NAND gate NAND0A thru/or NAND2A which considers current selector-signals ISEL1 as one input in the data creation circuit 232, for example, Inverter IV0A which reverses these outputs, respectively thru/or IV2A, NAND gate NAND0B which considers current selector-signals ISEL2 as one input or NAND2B, inverter IV0B which reverses these outputs, respectively, or IV2B is provided. The gradation data D0 is further inputted into NAND gate NAND0A and NAND0B, the gradation data D1 is further inputted into NAND gate NAND1A and NAND1B, and the gradation data D2 is further inputted into NAND gate NAND2A and NAND2B. And the data signal D0A thru/or D2A and D0B thru/or D2B are outputted, respectively from inverter IV0A thru/or IV2A and IV0B thru/or IV2B. However, this composition is an example, and if it can output the same signal, it is very good in other composition.
[0156]Next, operation of the semiconductor device for light-emitting displays concerning the 15th example constituted as mentioned above is explained. Drawing 25 is a timing chart which shows operation of the semiconductor device for light-emitting displays concerning the 15th example of this invention.
[0157]Since it begins to carry out the vertical scanning of the indicator 400 (refer to drawing 35), the period until the next vertical scanning starts is made into one frame. In the case of this example, two kinds of frames to which one side of the exclusive current selector signals ISEL1 and ISEL2 becomes high-level mutually appear by turns.
[0158]First, the 1st frame is explained. In current selector-signals ISEL1, in the 1st frame, high level and current selector-signals ISEL2 become a low level. In this case, in the output blocks 240a and 240b, by the 1st output block 240a into which the digital image data DA0 thru/or DA2 is inputted, and current is outputted. [switch SW1] On the other hand, in the 2nd output block 240b into which digital-image-data DB0 thru/or DB2 are inputted, switch SW2 turns off and current is memorized. In details, the 1-bit D/I converter 231 in the output block 240b memorizes any one of the reference current IR0 thru/or IR2, IG0 to IG2, IB0 to the IB2 more. However, in this frame, digital-gradation-data DB0 thru/or DB2 are in a low level, and switch SW1 of the 1-bit D/I converter 231 in the output block 240b has become OFF.
[0159]Next, the operation which memorizes the current of the output block 240b is explained.
[0160]With the start of the 1st frame, a pulse signal is inputted into F/F290c_1 of the 1st step as the start signal IST, Simultaneously with the input of this pulse signal, the shift register which comprises n F/F290 begins to operate in the clock signal ICL and the clock inversion signal ICLB being inputted into F/F290c_1. If output signal MSWB_of F/F290c_1 of 1st step 1 becomes high-level, the switches SW2 and SW3 of the 1-bit each D/I converter 231 of the output block 240b provided in the 1 output D/I converter 230e into which this output signal MSWB_1 is inputted will serve as one. If the switches SW2 and SW3 are turned on, since between the gate drain short-circuits, TFTT1 for current memory / output in the 1-bit D/I converter 231 will operate in a saturation region. And where this operation is stabilized, according to the current capability of TFTT1, the gate voltage is set up so that reference current may flow between the drain sauce of TFTT1.

[0161]After being in a stable state, signal MSWB_1 is set to a low level, and. If output signal MSWB_2 of F/F of the 2nd step becomes high-level, the switches SW2 and SW3 in the output block 240b provided in the 1 output D/I converter 230e in the RGB D/I converter 220d in which F/F 290_1 was formed will serve as OFF. At this time, the gate voltage of TFTT1 of the output block 240b in the RGB D/I converter 220d in which F/F 290_1 was formed is held at the voltage that reference current flows by the capacitative element C1. As a result, it is not concerned with each current capability, but reference current is memorized by TFTT1. Such a signal municipal solid waste makes a high-level period 3 output-current storage duration in the RGB D/I converter 220d. On the other hand, the switches SW2 and SW3 of the output block 240b in the RGB D/I converter 220d in which F/F of the 2nd step was provided serve as one, and in the state where it was stabilized. It operates in a saturation region so that reference current may flow between the drain sauce of TFTT1 of the 1-bit D/I converter 231, and according to the current capability of TFTT1, gate voltage is set up so that the reference current may flow.
[0162]In the 1st frame period, the above 3 output-current storage duration is repeated about the 2nd output block 240b in all the RGBD/I converters 220d, and reference current is memorized by the 2nd output block 240b of all the 1 output D/I converters 230e.
[0163]Next, operation of the 1st output block 240a in the 1st frame is explained. With the 1st frame, the vertical scanning circuit 300 chooses the control line of one line at a time. The scanning pulse Y_1 which is the 1st line and 2nd-line output, and Y_2 are shown in drawing 25.
[0164]If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1st output block 240a in the 1 output D/I converter 230e for every output synchronizing with this. If the digital gradation data D0 thru/or D2 is inputted, according to these levels (the high level (H) / low level (L)), ON and OFF of switch SW1 in the 1-bit D/I converter 231 will be controlled, The current memorized by TFTT1 in the current driving period of the last frame is outputted, and gray scale representation is performed.
[0165]As shown in Table 1, an output current value can be adjusted with the digital gradation data inputted from 0 to 7xi0. Since gate voltage is set up so that current equivalent to a reference current source may flow according to the current capability of TFTT1 with the last frame, and it is outputting using the TFTT1 [same], regardless of current capability dispersion, dispersion in output current is small and high accuracy is obtained.
[0166]On the other hand, in the 1st frame, the output MSWA of a shift register is always a low level, and the switches SW2 and SW3 in all the output blocks 240a are still OFF always.
[0167]In the 2nd following frame, operation of the 1st output block 240a and operation of the 2nd output block 240b are replaced by making high-level a low level and current selector-signals ISEL2 for current selector-signals ISEL1. As a result, the 1st output block 240a memorizes current, and the 2nd output block 240b outputs current.
[0168]By repeating the above operation every two frames, this example can supply highly precise current to a pixel circuit. In this example, since two output blocks are provided in one output, in each frame, since current is outputted, one output block is used, and the output block of another side can be used in order to memorize current, and does not independently need to provide current storage duration. Thereby, all 1 frame periods turn into a current driving period, and it becomes possible to secure charge and discharge time, such as load which wiring to the pixel in an indicator has, for a long time. Therefore, the current of still higher accuracy can be supplied to a pixel.
[0169]To the 15th example, the 2nd thru/or the 14th example may be applied and the same effect can be acquired.
[0170]The cycle of current memory will not be limited for every frame, and may be every several frames.Since the period of current memory becomes long by carrying out the cycle of current memory every several frames, current can be memorized in still higher accuracy. However, it is needed for the gate voltage corresponding to the current at the time of memory for the change below the accuracy called for by leak of a transistor, etc. not to arise.
[0171]Next, the 16th example of this invention is described. The 16th example establishes a precharge circuit in the latter part of a 1 output D/I converter. Drawing 26 is a block diagram

showing the composition of the semiconductor device for light-emitting displays concerning the 16th example of this invention.
[0172]The D/I converter 210e is formed in the 16th example. The D/I converter 210e has the same composition as the D/I converter 210d in the 16th example except for the point that the precharge circuit 250 is established in the latter part of the one output each D/I converter 230e, respectively. A precharge signal PC input is carried out in the precharge circuit 250.
[0173]the period when the precharge circuit 250 is set up by a precharge signal -- each output **** of the D/I converter 210d -- the voltage decided by the output current of the 1 output D/I converter is outputted instead of the output current of the 1 output D/I converter 230e. Drawing 27 is a circuit diagram showing the example of composition of the precharge circuit 250. The N channel transistors T31 thru/or T33 and the P channel transistor T34 which are controlled by precharge signal PC are provided in the precharge circuit 250. The output current IOUT from the 1 output D/I converter 230e is inputted into one end of the transistors T31 and T32, and the non-inversed input terminal of the dummy load circuit 252 and the operational amplifier 251 is connected to the other end of the transistor T31. In the false addition circuit 252, one end of the transistor T33 is connected to the transistor T31, and the gate of the P channel transistor T35 is connected to the other end of the transistor T33. The voltage VEL is supplied to the sauce of the transistor T35, and the other end is connected to the transistor T31. The output signal of operational amplifier 251 the very thing is inputted into the inversed input terminal of the operational amplifier 251, one end of the transistor T32 is connected to the output terminal of the operational amplifier 251, and the other end is connected to the other end of the transistor T34. The driving current of a light emitting device is outputted from the common node of the transistors T32 and T34.
[0174]In such a precharge circuit 250, it is determined whether for the output current IOUT of the 1 output D/I converter 230e to be made into the output current Iout, and to carry out a direct output with the transistor T34, or output to the dummy load circuit 252. It is determined by the transistor T32 whether the output of the operational amplifier 251 is considered as the output of the D/I converter 210e. Since the operational amplifier 251 is carrying out negative feedback of the output to the inversion input, it carries out the voltage follower output of the voltage inputted into a noninverting input. The transistor T35 is the same transistor as TFTT102 of the pixel circuit (drawing 38 (a)) in the indicator 400, or a transistor which has equivalent current capability. However, it is good also as composition which short-circuits between the gate drains of the transistor T35, and does not form the transistor T33 as the dummy load circuit 252. The transistor T31, T32, and T34, If it has composition which can also consider it as a reverse polar transistor, and inputs the precharge signal PC itself and its inversion signal, for example with some polarity of precharge signal PC in order to act as a switch, it is also possible to use what kind of polar transistor.
[0175]Next, operation of the precharge circuit 250 is explained. Drawing 28 is a timing chart which shows operation of the precharge circuit 250.
[0176]In this example, an one-line selection period is divided into the 1st period and 2nd period by the level of precharge signal PC.
[0177]In the 1st period, precharge signal PC has become high-level, and it is a precharge period. If the scanning pulse Y_1 becomes high-level, the control line of the 1st line will be chosen and the triplet digital gradation data D0 thru/or D2 of the 1st line for several output minutes will be inputted into the 1 output D/I converter 230e for every output synchronizing with this. The 1 output D/I converter 230e outputs current according to the relation shown in Table 1 from the inputted digital gradation data DA0 thru/or DA2. If precharge signal PC serves as a high bell at this time, the transistor T34 in the precharge circuit 250 will serve as OFF, and the transistors T31 and T32 will serve as one. Therefore, in the precharge circuit 250, the output current of the 1 output D/I converter 230e flows into the dummy load circuit 252. Since the transistor T35 is formed in the dummy load circuit 252, when the output current Iout is stabilized and it flows, the gate voltage of the transistor T35 turns into gate voltage when the output current Iout stabilized and flows into the pixel circuit in an indicator, and the almost same voltage. And this voltage serves as an input of the voltage follower constituted by the operational amplifier 252, and in this

precharge period, since the transistor T32 serves as one, the output of a voltage follower turns into an output of the D/I converter 210e. Therefore, in this period, the gate voltage of the transistor T35 can be impressed to the pixel circuit in an indicator.
[0178]Since the dummy load circuit 252 has the wiring load very smaller than a pixel circuit etc. which need to be and carry out charge and discharge near the 1 output D/I converter 230e, At very high speed, operation of stabilizing and sending the fixed output current of the 1 output D/I converter 230e through the transistor T35 can be performed, even when an output current value is low as compared with the case where the pixel circuit in an indicator is driven by the fixed output current of a 1 output D/I conversion circuit. Since operation of impressing the gate voltage of the transistor T35 to the pixel circuit in an indicator is also performed with the output of low impedance called a voltage follower, it is realizable at high speed.
[0179]Precharge signal PC serves as a low level, and the 2nd period is a current output period. When precharge signal PC serves as a low level, the transistor T34 in the precharge circuit 250 serves as one, and the transistors T31 and T32 serve as OFF. Therefore, in the precharge circuit 250, the output current of the 1 output D/I converter 230e is outputted as it is, and the pixel circuit in an indicator drives. Since precharge operation is performed in the 1st period at this time, when the output current of the 1 output D/I converter 230e is stabilized and it flows, near voltage is impressed to the pixel circuit in an indicator. Therefore, in the 2nd period, operation of amending current capability dispersion between transistor TFTT102 (drawing 38 (a)) in the pixel circuit in the transistor T35 and an indicator, and operation of it being stabilized in the pixel circuit in an indicator, and driving the output current Iout to it are performed. As a result, the quantity which carries out the charge and discharge of the wiring load etc. in the 2nd period is small, and ends. Therefore, the 2nd period can shorten a period compared with the case where precharge operation is not performed. After outputting stable voltage by precharge operation, it can operate without being influenced by the state in front of an one-line selection period in order to perform a current drive.
[0180]Then, in the scanning pulse Y_1, a low level and the scanning pulse Y_2 become high-level, the control line of the 2nd line is chosen, and the same operation is repeated. By the above operation, the pixel circuit in an indicator can be driven at high speed by the current of still higher accuracy.
[0181]The same effect can be acquired even if it applies, when the circuit and the semiconductor device which may apply the 1st thru/or the 15th example as a 1 output D/I converter of the 16th example, and supplies current are not contained in this invention.
[0182]Next, the 17th example is described. The 17th example changes the composition of the precharge circuit in the 16th example. Drawing 29 is a block diagram showing the composition of the precharge circuit in the 17th example of this invention.
[0183]In addition to the component of the precharge circuit 250, the N channel transistor T36 and the P channel transistors T37 and T38 into which precharge signal PC is inputted are provided in the precharge circuit 250a in the 17th example. The transistor T38 is connected between the output terminal of the operational amplifier 251, and the inversed input terminal. The capacitative element C3 is inputted into the output terminal of the operational amplifier 251, the transistor T36 is connected between the other end and inversed input terminal, and the transistor T37 is connected between non-inversed input terminals.
[0184]The precharge circuit 250a constituted in this way, By having a circuit which cancels the offset voltage of the operational amplifier 251 known well, and performing offset cancellation operation at a current driving period, it cannot be influenced by the offset voltage of the operational amplifier 251, but precharge operation can be performed. Other operations are the same as operation of the precharge circuit 250 in the 16th example.
[0185]Next, the 18th example of this invention is shown in drawing 32. The data register 203 in which the 18th example holds the digital data signal inputted, The shifting-data register 202 which outputs the scanning signal which synchronized with the timing to hold, It is the horizontal drive circuit 200 provided with the data latch 204 which holds the signal of all the data registers synchronizing with a latch signal, and is outputted to the D/I converter 210, and the D/I converter 210 which outputs current according to a digital data signal. The D/I converter 210

may also include a precharge circuit. The D/I converter 210 may comprise a D/I converter of the example of either [this invention] the 1st thru/or the 17th either.
[0186]Next, the 19th example of this invention is shown in drawing 33. The 19th example can increase the data line and the pixel circuit which can be driven without the output of the D/I converter 210 of the 18th example being having enabled it to connect with the data line of two or more indicators 400 one by one, and increasing circuit structure by the selector circuit 211.
[0187]Next, the 20th example of this invention is shown in drawing 34. The 20th example builds the reference current source 212 which creates reference current in the 18th example in the horizontal drive circuit 200.
[0188]In the 1st of this invention thru/or the example of 20, although TFT explains the transistor, it may comprise a more general transistor and two or more horizontal drive circuits 200 may be used to one indicator. The indicator 400, the horizontal drive circuit 200, and the vertical scanning circuit 300 may be formed on the same substrate by creating all the transistors by TFT. In this case, highly precise precharge is realizable by creating the load of the indicator 400, and the load (circuit) of the same composition for the load (circuit) of the precharge circuit in the example of this invention.
[0189]Although the 1st of this invention thru/or the example of 20 explain the example driven by 4096 color specification as which 0 gradation - the triplet digital gradation data of 7 gradation displays input the light-emitting display provided with the light emitting device whose current-luminance property is proportionality in the color (R, G, B), respectively, A monochromatic case or the more nearly same composition also in the case of a multi-bit is extensible as it is. Although all transistors are set to TFT, this invention is realizable by same composition also with a more general transistor. Although drawing 38 (a) is assumed as a pixel circuit of an active matrix system, this invention is [as opposed to / other pixels of a simple matrix system or pixel circuits of a current drive system / again] realizable by same composition.
[0190]The above examples are applied also to a current load device provided with a more general current load device, although it is explaining in a light-emitting display provided with a light-emitting display device.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the composition of the semiconductor device for a current load device drive concerning the 1st example of this invention.
[Drawing 2]It is a block diagram showing the composition of the 1 output D/I converter 230.
[Drawing 3]It is a block diagram showing the composition of the 1-bit D/I converter 231.
[Drawing 4]It is a timing chart which shows operation of the semiconductor device for a current load device drive concerning the 1st example of this invention.
[Drawing 5]It is a block diagram showing the composition of the 1-bit D/I converter in the 2nd example of this invention.
[Drawing 6]It is a block diagram showing the composition of the 1-bit D/I converter in the 3rd example of this invention.
[Drawing 7]It is a block diagram showing the composition of the 1-bit D/I converter in the 4th example of this invention.
[Drawing 8]It is a block diagram showing the composition of the 1-bit D/I converter in the 5th example of this invention.
[Drawing 9]It is a block diagram showing the composition of the 1-bit D/I converter in the 6th example of this invention.
[Drawing 10]It is a block diagram showing the composition of the semiconductor device for light-emitting displays concerning the 7th example of this invention.
[Drawing 11]It is a block diagram showing the composition of the 1 output D/I converter 230a.
[Drawing 12]It is a block diagram showing the composition of the 1-bit D/I converter 231f.
[Drawing 13]It is a timing chart which shows operation of the semiconductor device for a current load device drive concerning the 7th example of this invention.
[Drawing 14]It is a block diagram showing the composition of the 1-bit D/I converter in the 8th example of this invention.
[Drawing 15]It is a block diagram showing the composition of the semiconductor device for a current load device drive concerning the 9th example of this invention.
[Drawing 16]It is a block diagram showing the composition of the 1 output D/I converter 230b.
[Drawing 17]It is a block diagram showing the composition of the 1-bit D/I converter 231h.
[Drawing 18]It is a block diagram showing the composition of the 1-bit D/I converter in the 10th example of this invention.
[Drawing 19]It is a block diagram showing the composition of the semiconductor device for a current load device drive concerning the 13th example of this invention.
[Drawing 20]It is a block diagram showing the composition of the 1 output D/I converter 230c.
[Drawing 21]It is a block diagram showing the composition of the 1-bit D/I converter in the 14th example of this invention.
[Drawing 22]It is a block diagram showing the composition of the semiconductor device for a current load device drive concerning the 15th example of this invention.
[Drawing 23]It is a block diagram showing the composition of the 1 output D/I converter 230e.
[Drawing 24]It is a circuit diagram showing the composition of an example of the data creation circuit 232.

[Drawing 25]It is a timing chart which shows operation of the semiconductor device for a current load device drive concerning the 15th example of this invention.
[Drawing 26]It is a block diagram showing the composition of the semiconductor device for a current load device drive concerning the 16th example of this invention.
[Drawing 27]It is a circuit diagram showing the composition of the precharge circuit 250.
[Drawing 28]It is a timing chart which shows operation of the precharge circuit 250.
[Drawing 29]It is a block diagram showing the composition of the 1-bit D/I converter in the 17th example of this invention.
[Drawing 30]It is a block diagram showing the composition of the 1-bit D/I converter in the 11th example of this invention.
[Drawing 31]It is a block diagram showing the composition of the 1-bit D/I converter in the 12th example of this invention.
[Drawing 32]It is a block diagram showing the composition of the semiconductor device for a current load device drive concerning the 18th example of this invention.
[Drawing 33]It is a block diagram showing the composition of the semiconductor device for a current load device drive concerning the 19th example of this invention.
[Drawing 34]It is a block diagram showing the composition of the semiconductor device for a current load device drive concerning the 20th example of this invention.
[Drawing 35]The light emitting device as which luminosity is determined by the current supplied is a figure showing the composition of the light-emitting display in each pixel.
[Drawing 36]It is a circuit diagram showing the composition of one pixel display part in the case of simple matrix driving.
[Drawing 37]It is a circuit diagram showing the composition of one pixel display part in an active-matrix drive.
[Drawing 38](a) And (b) is a circuit diagram showing other composition of one pixel display part in an active-matrix drive.
[Drawing 39]It is a block diagram showing an example of the composition of the horizontal drive circuit 200 for outputting current to the indicator 400.
[Drawing 40]It is a circuit diagram showing the 1st conventional example of digital one / current conversion part for one output.
[Drawing 41]It is a circuit diagram showing the 2nd conventional example of digital one / current conversion part for one output.
[Description of Notations]
210, 210a - a 210 d:D/I converter
220, 220a - a 220 c:RGB D/I converter
230, 230a - a 230c:1 output D/I converter (1 output D/I conversion circuit)
231, 231a - a 231 i:1-bit D/I converter (1-bit D/I conversion circuit)
250 250a: Precharge circuit

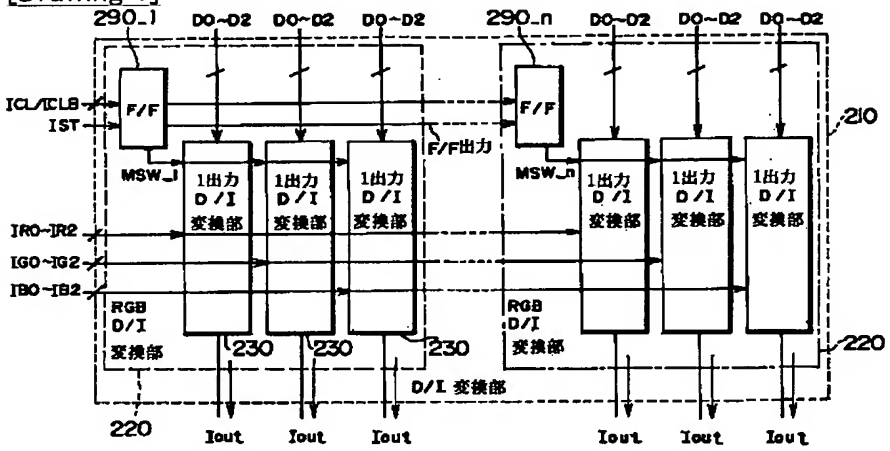
[Translation done.]

* NOTICES *

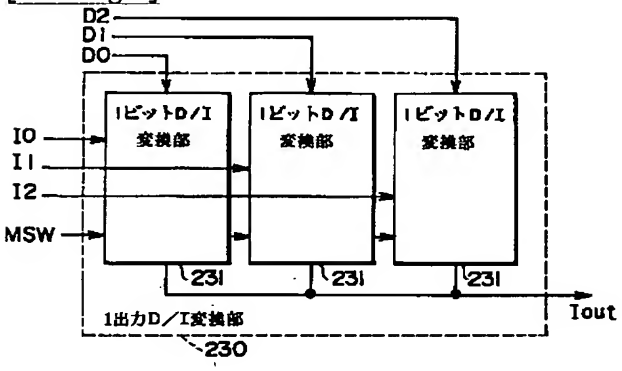
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

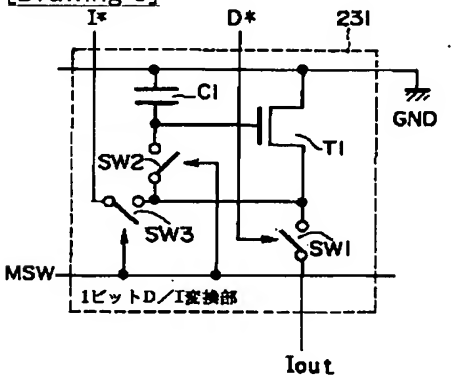
[Drawing 1]



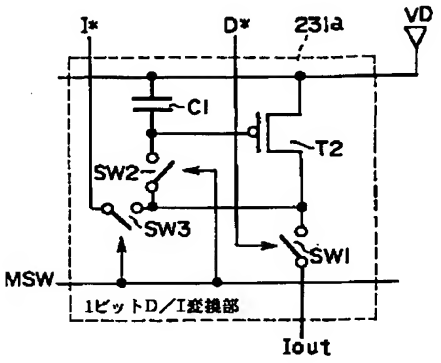
[Drawing 2]



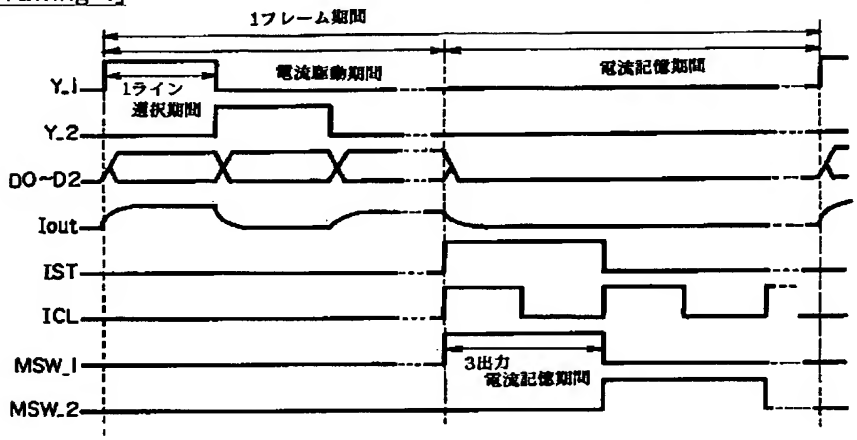
[Drawing 3]



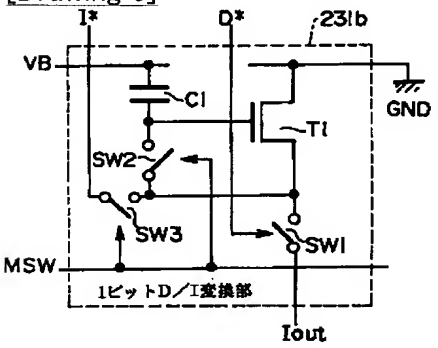
[Drawing 5]



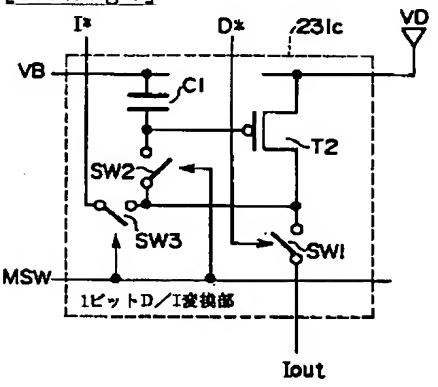
[Drawing 4]



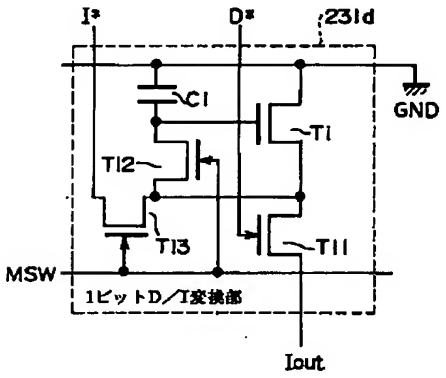
[Drawing 6]



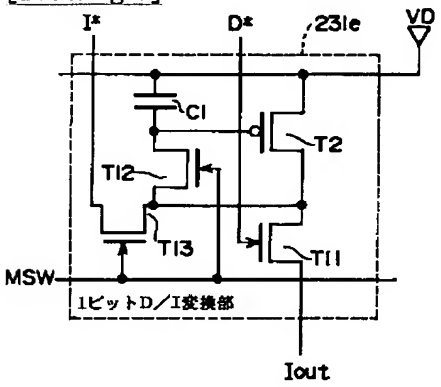
[Drawing 7]



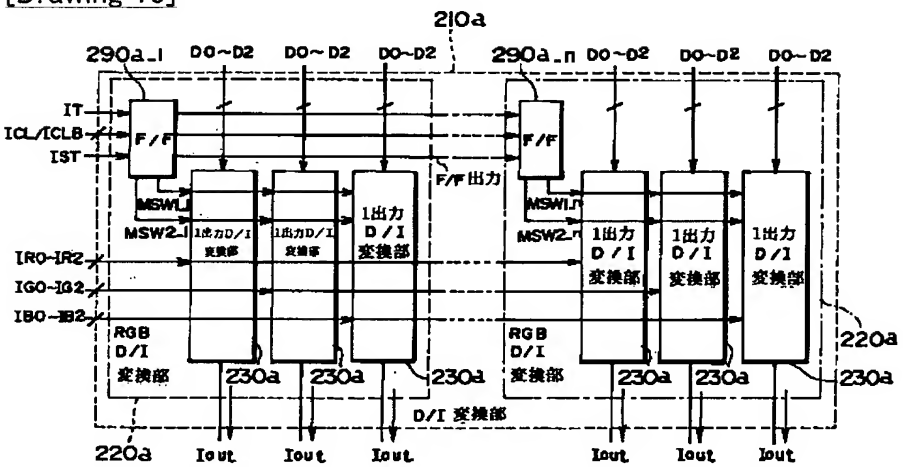
[Drawing 8]



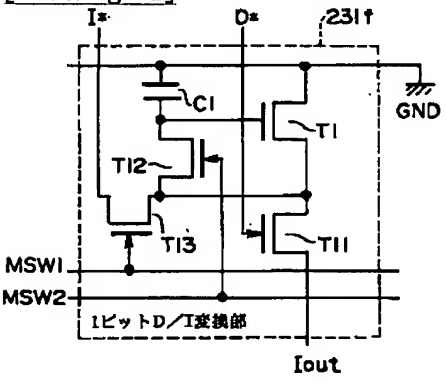
[Drawing 9]



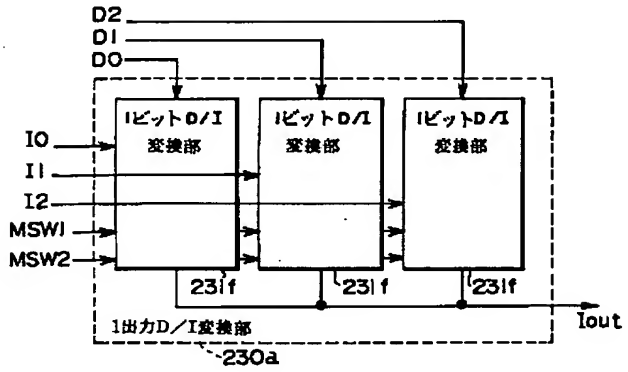
[Drawing 10]



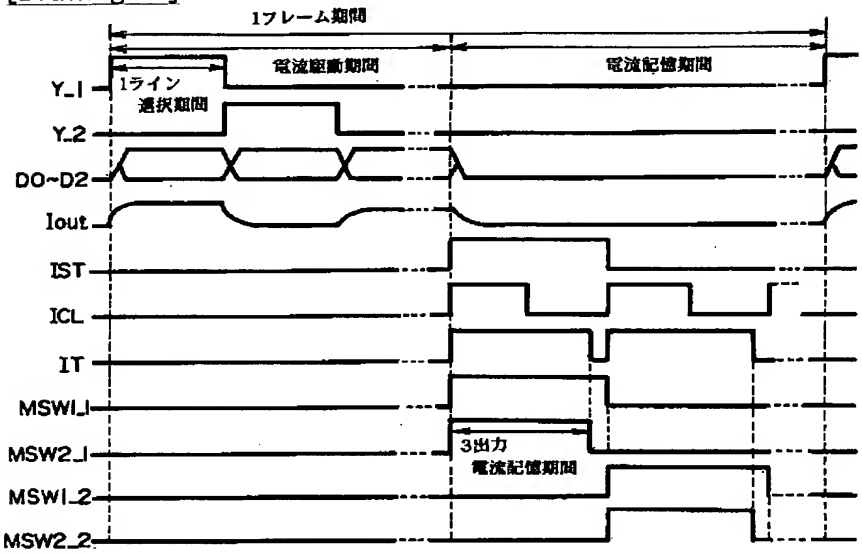
[Drawing 12]



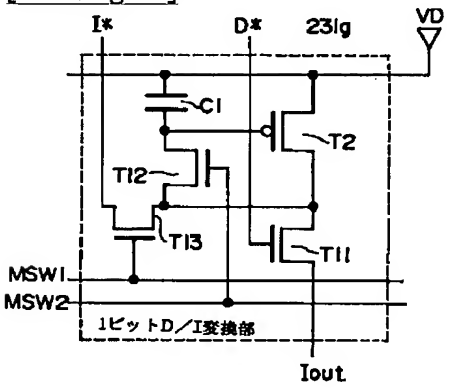
[Drawing 11]



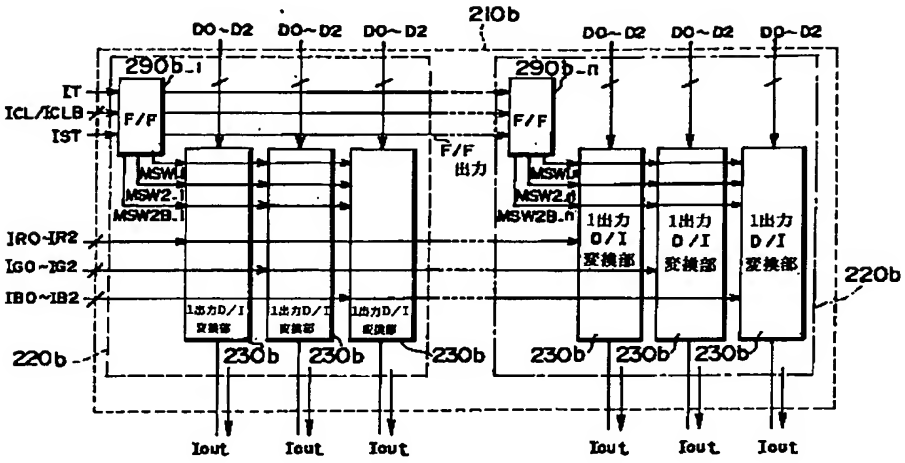
[Drawing 13]



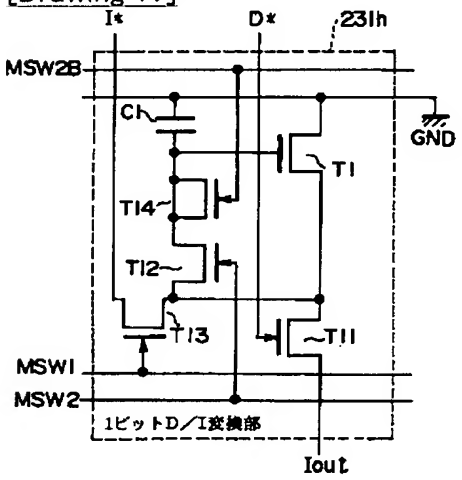
[Drawing 14]



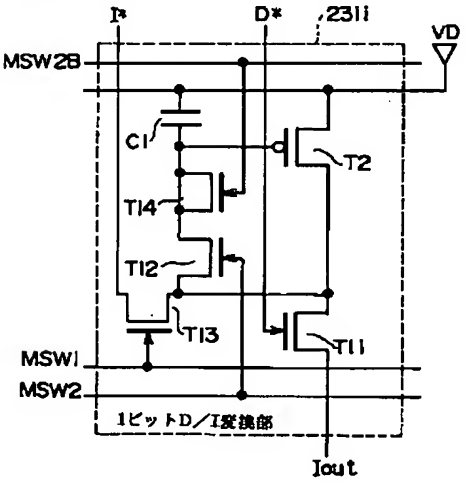
[Drawing 15]



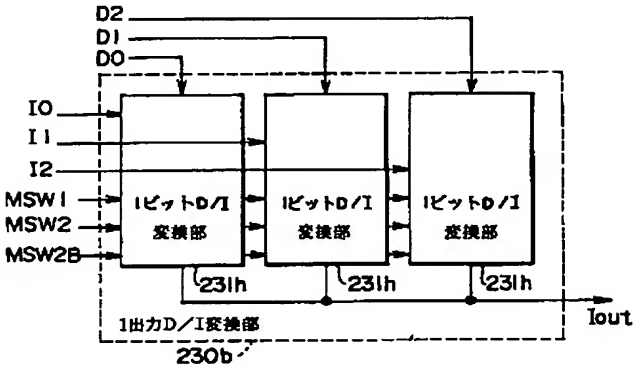
[Drawing 17]



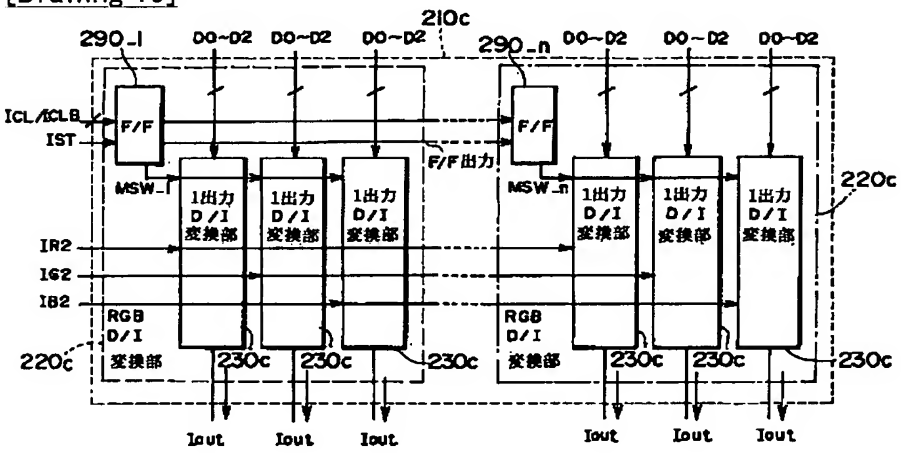
[Drawing 18]



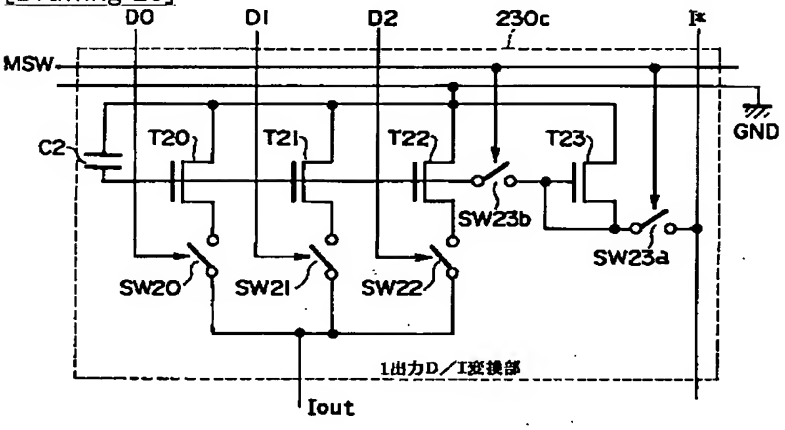
[Drawing 16]



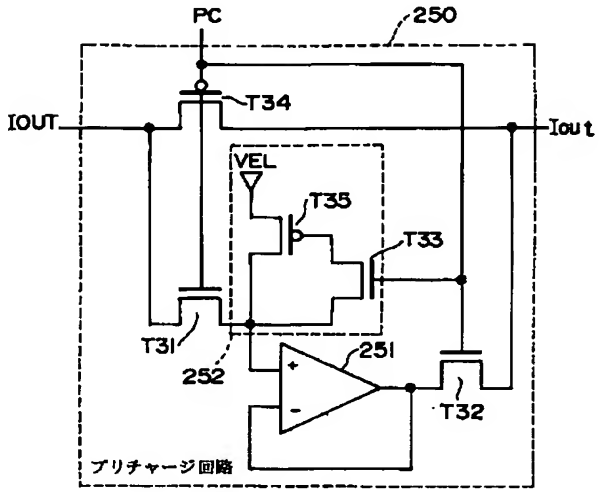
[Drawing 19]



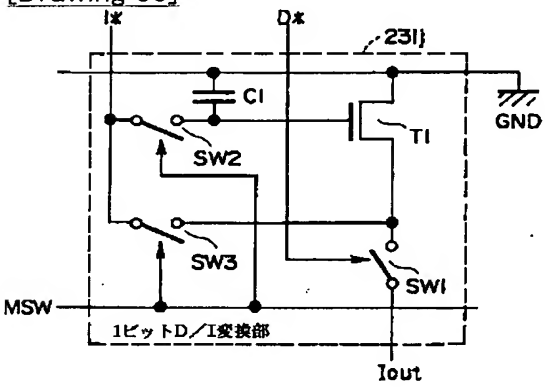
[Drawing 20]



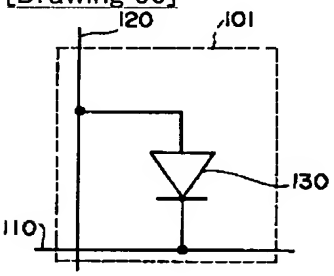
[Drawing 27]



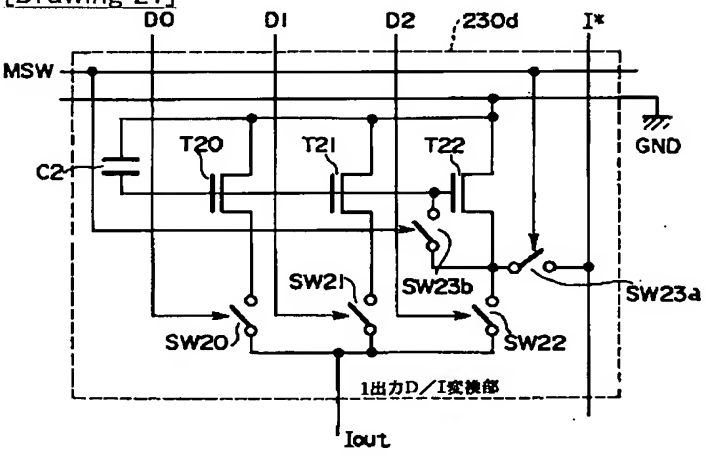
[Drawing 30]



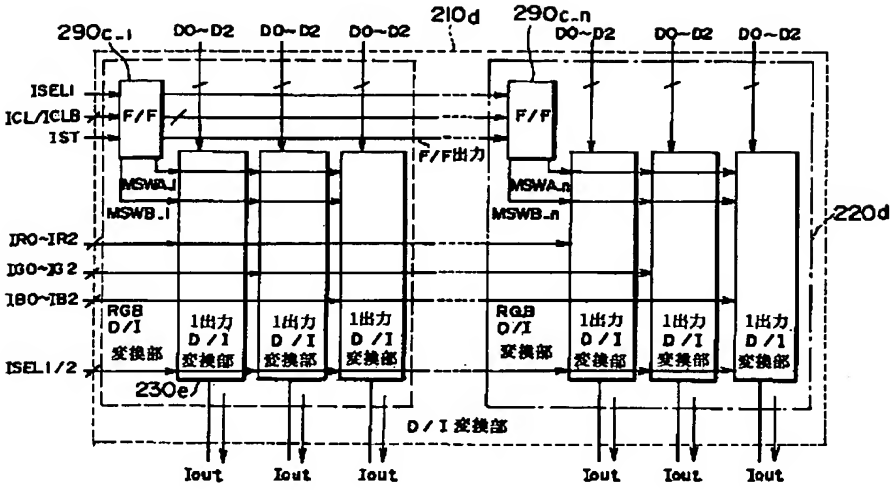
[Drawing 36]



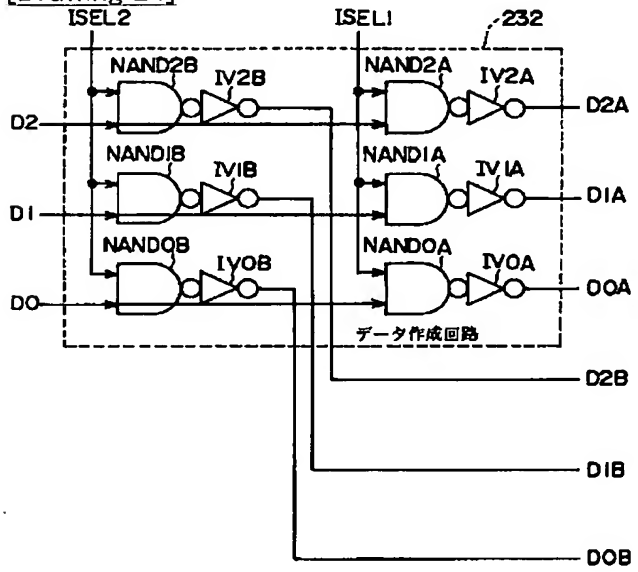
[Drawing 21]



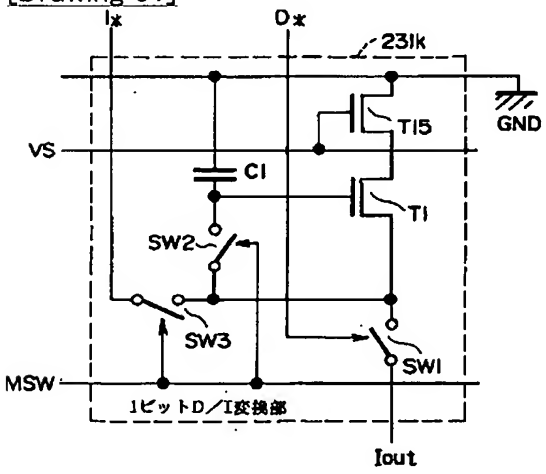
[Drawing 22]



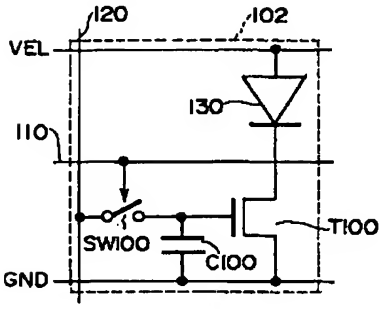
[Drawing 24]



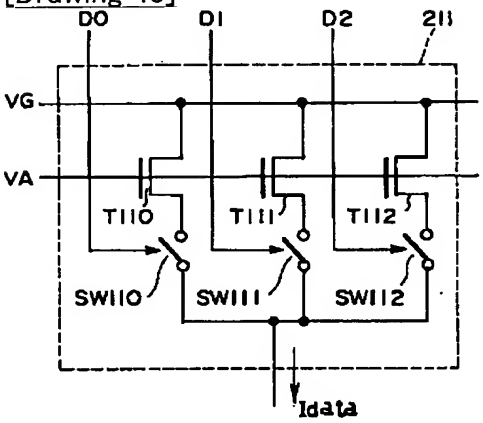
[Drawing 31]



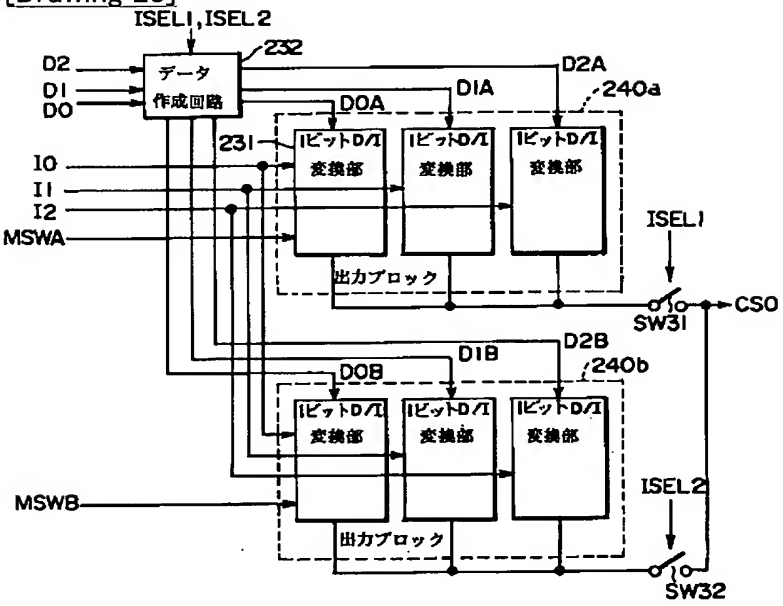
[Drawing 37]



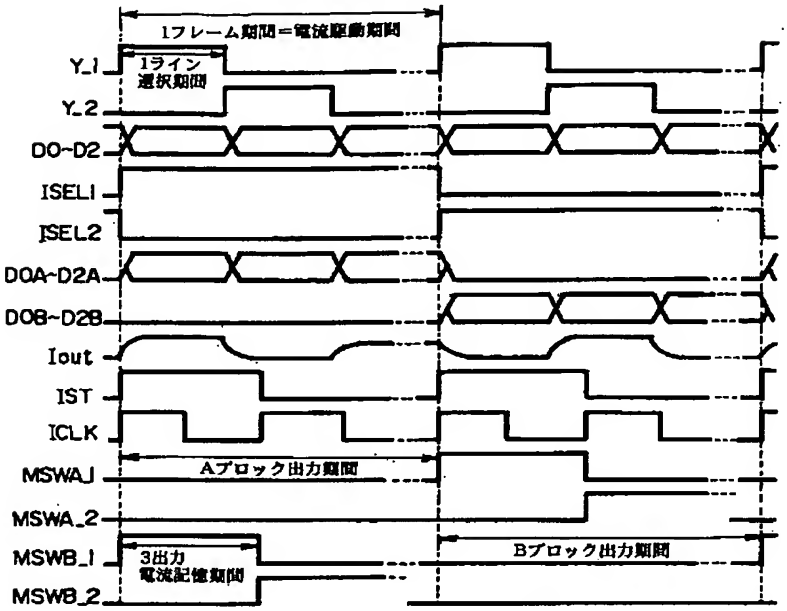
[Drawing 40]



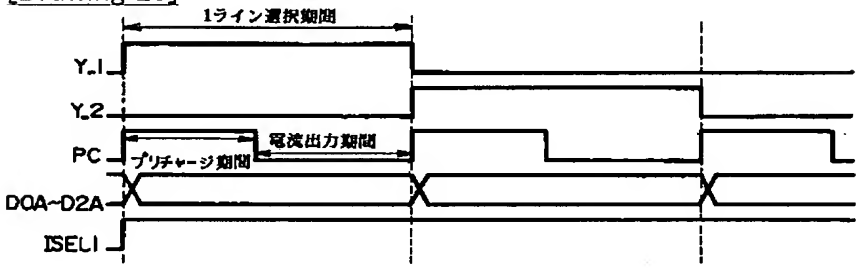
[Drawing 23]



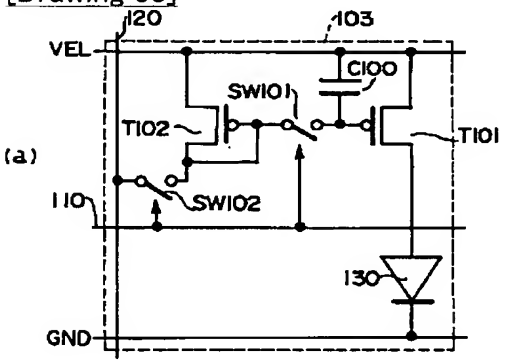
[Drawing 25]

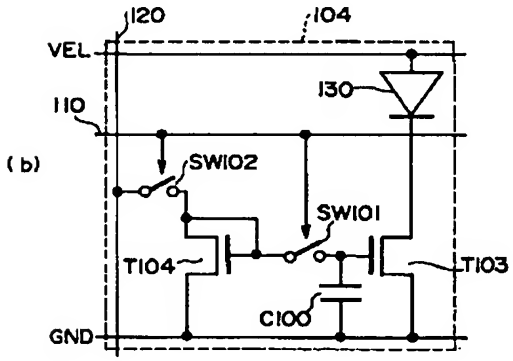


[Drawing 28]

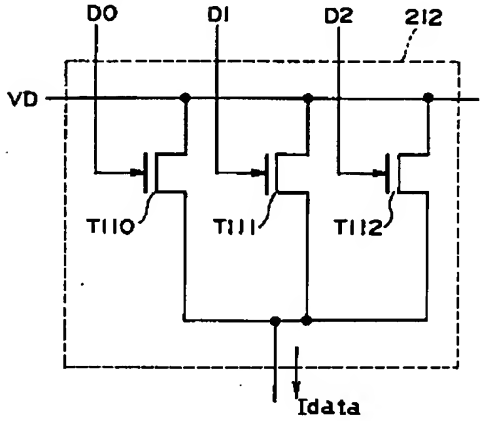


[Drawing 38]

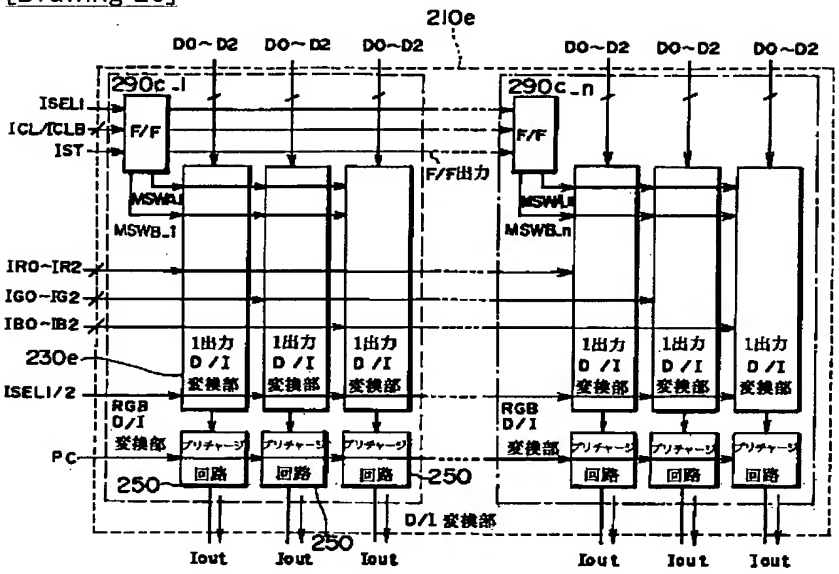




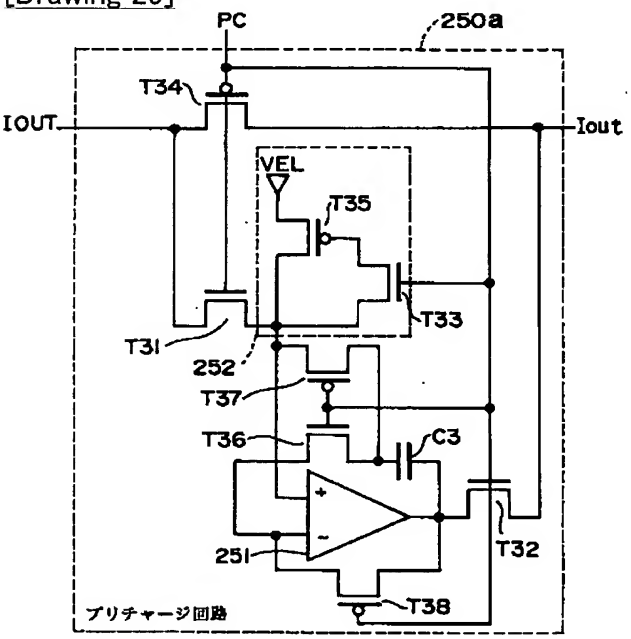
[Drawing 41]



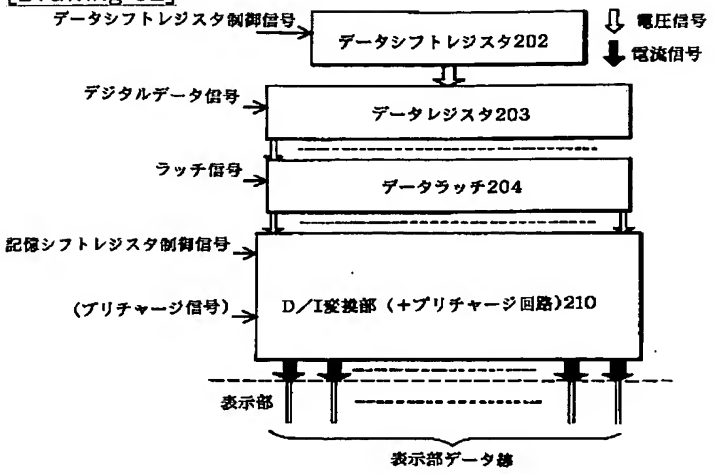
[Drawing 26]



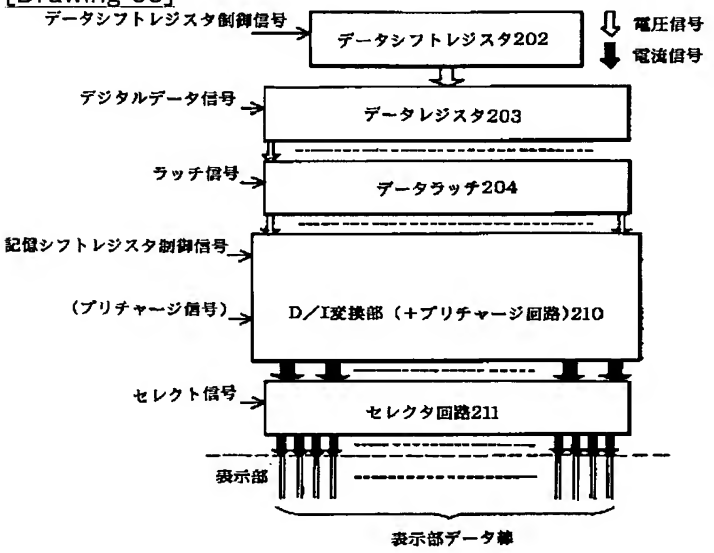
[Drawing 29]



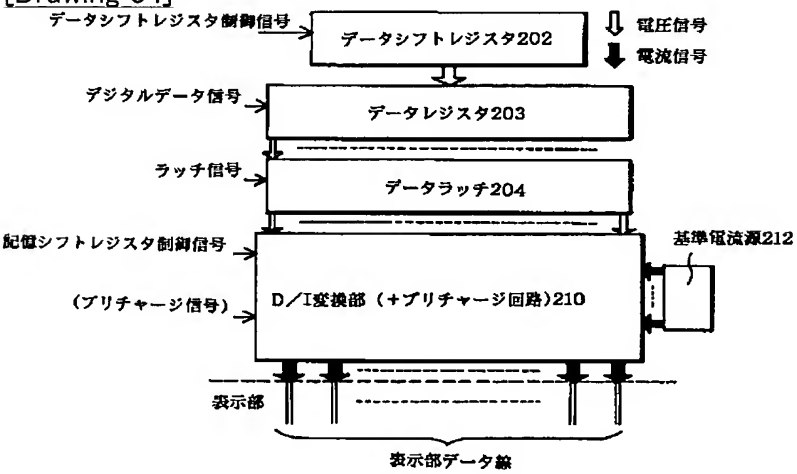
[Drawing 32]



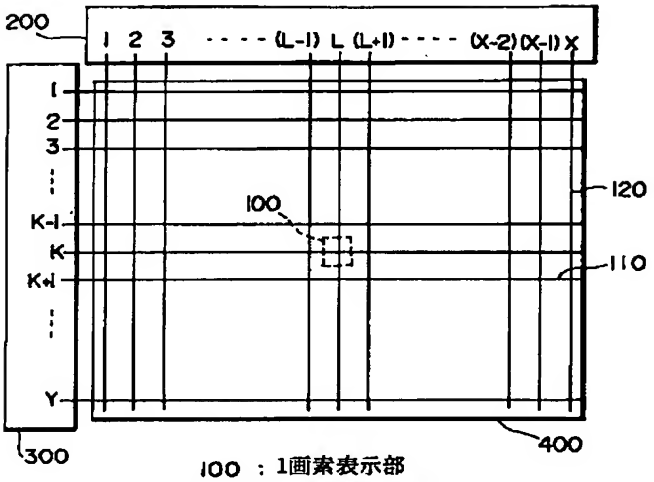
[Drawing 33]



[Drawing 34]

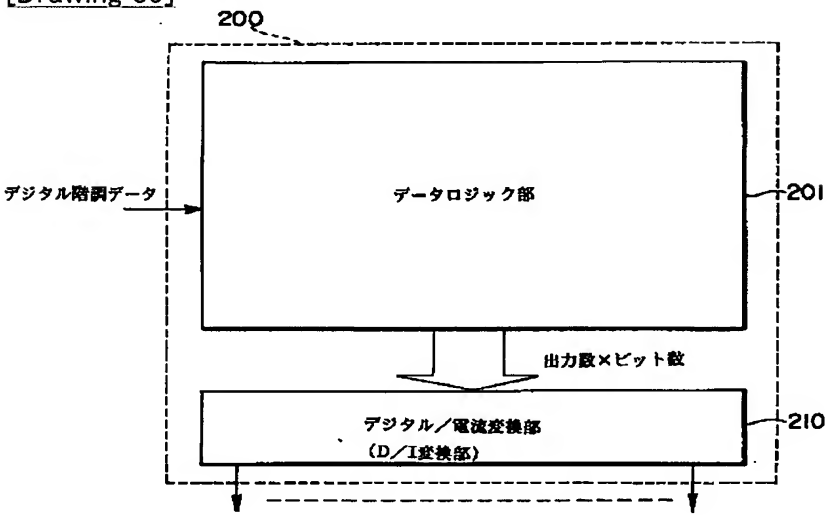


[Drawing 35]



100 : 1画素表示部
200 : 水平駆動回路
300 : 垂直走査回路
400 : 表示部

[Drawing 39]



[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号
特開2003－195812
（P2003－195812A）
(43)公開日　平成15年７月９日(2003.7.9)

(51)Int.Cl.⁷		識別記号	FI		テーマコード（参考）
Ｇ０９Ｇ	3/30		Ｇ０９Ｇ	3/30	Ｊ　５Ｃ０５８
	3/20	６１１		3/20	６１１Ｈ　５Ｃ０８０
		６１２			６１２Ｆ
		６２１			６２１Ｍ
		６２３			６２３Ｂ

審査請求　未請求　請求項の数53　ＯＬ　（全 35 頁）　最終頁に続く

(21)出願番号　特願2002－252191(P2002－252191)
(22)出願日　平成14年８月29日(2002.8.29)
(31)優先権主張番号　特願2001－259677(P2001－259677)
(32)優先日　平成13年８月29日(2001.8.29)
(33)優先権主張国　日本（ＪＰ）

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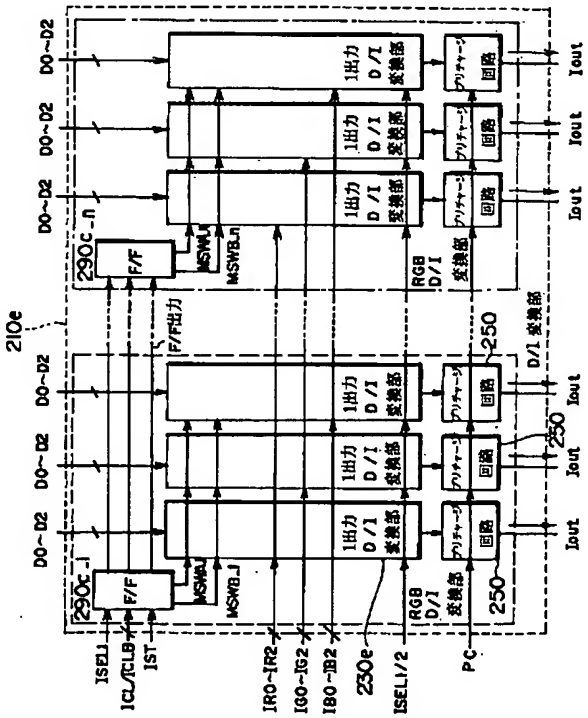
東京都港区芝五丁目７番１号　日本電気株式会社内
(74)代理人　100090158
弁理士　藤巻　正憲

Ｆターム(参考)　5C058 AA12 BA01 BB25
5C080 AA06 BB05 BB06 CC03 DD05
DD08 EE29 FF11 FF12 JJ02
JJ03 JJ04

(54)【発明の名称】　電流負荷デバイス駆動用半導体装置及びそれを備えた電流負荷デバイス

(57)【要約】
【課題】　入力されるデジタル画像データに対し、精度の高い出力電流を供給することができ、出力電流値が低い場合でも高速で電流負荷デバイスを駆動することができる。
【解決手段】　発光表示装置駆動用半導体装置のＤ／Ｉ変換部２１０ｅにおいては、各１出力Ｄ／Ｉ変換部２３０ｅの後段に、夫々プリチャージ回路２５０が設けられている。プリチャージ回路２５０には、プリチャージ信号ＰＣ入力される。Ｄ／Ｉ変換部２３０ｅは、内部に２つ出力ブロックを有し、１フレームごとに電流を記憶、出力するという役割を変えることで画素を駆動する期間を長く確保することができる。また、駆動時には、プリチャージ回路２５０にて、出力電流に対応する電圧を画素に印加した後に、電流駆動を行うため、高速に画素を駆動できる。



【特許請求の範囲】

【請求項１】　電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、
入力される１種又は複数種の基準電流により決定されるｎ（ｎは自然数）種の電流値を記憶する機能と、前記記憶電流値から得られる２ｎレベルの電流値の内、入力されるｎビットデジタルデータに従って１つの電流を出力する機能を備えるｎビットデジタル／電流変換回路を、１つ又は複数の前記セルへの供給端子毎に少なくとも一つ備えることを特徴とする電流負荷デバイス駆動用半導体装置。

【請求項２】　前記基準電流は、前記電流負荷デバイス駆動用半導体装置内にある基準電流生成回路により得られることを特徴とする請求項１に記載の電流負荷デバイス駆動用半導体装置。

【請求項３】　前記ｎビットデジタル／電流変換回路に、前記電流記憶時には電流が出力しないデジタルデータを伝え、電流出力時には目的の動作に対応した電流を出力するデジタルデータを伝える回路を備えることを特徴とする請求項１又は２に記載の電流負荷デバイス駆動用半導体装置。

【請求項４】　前記ｎビットデジタル／電流変換回路は、１種の基準電流より１種の電流値を記憶し、入力される１ビットデジタルデータにより前記記憶電流を出力するか否かを決める１ビットデジタル／電流変換回路をｎ個備えることを特徴とする請求項１乃至３のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項５】　前記１ビットデジタル／電流変換回路は、前記基準電流の電流値を記憶することを特徴とする請求項４に記載の電流負荷デバイス駆動用半導体装置。

【請求項６】　ｎ個の前記基準電流の電流値の比は、最も低い電流値から順次２倍したものに設定されており、前記ｎビットデジタル電流変換回路は、ｎ個の前記１ビットデジタル／電流変換回路の出力を並列に接続したものを前記ｎビットデジタル／電流変換回路の出力とすることで、ｎビットデジタルデータに従って、２ｎレベルの電流値を出力することができることを特徴とする請求項４又は５に記載の電流負荷デバイス駆動用半導体装置。

【請求項７】　前記１ビットデジタル／電流変換回路は、前記基準電流が流れる信号線と、前記デジタル画像データの１ビットが伝達されるデータ線と、第１及び第２の制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された第１のトランジスタと、前記トランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、前記第１のトランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号により制御される第１のスイッチと、前記第１のトランジスタのゲートと前記第１のトランジスタのドレイン又は前記信号線との間に接続され前記第２の制御線を伝達する信号により制御される第２のスイッチと、前記第１のトランジスタのドレインと前記信号線との間に接続され前記第１の制御線を伝達する信号により制御される第３のスイッチと、を有することを特徴とする請求項４乃至６のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項８】　前記１ビットデジタル／電流変換回路は、前記基準電流が流れる信号線と、前記デジタル画像データの１ビットが伝達されるデータ線と、制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された第１のトランジスタと、前記第１のトランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、前記第１のトランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号により制御される第１のスイッチと、前記第１のトランジスタのゲートと前記１のトランジスタのドレイン又は前記信号線との間に接続され前記制御線を伝達する信号により制御される第２のスイッチと、前記トランジスタのドレインと前記信号線との間に接続され前記制御線を伝達する信号により制御される第３のスイッチと、を有することを特徴とする請求項４乃至６のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項９】　前記第１のトランジスタのソースと前記第１の電圧供給線の間に、ゲートが第３の電圧供給線によりバイアスされている第２のトランジスタを追加された前記１ビットデジタル／電流変換回路を備えることを特徴とする請求項７又は８に記載の電流負荷デバイス駆動用半導体装置。

【請求項１０】　前記第１のスイッチがオフ状態で前記第２及び第３のスイッチがオン状態のときに、前記トランジスタは、そのゲートードレイン間が短絡されて飽和領域で動作し、その動作が安定した段階における前記トランジスタのゲートーソース間電圧は、前記基準電流をドレインーソース間に流すために必要な電圧となり、その値は前記トランジスタの電流能力に従い決定され、前記トランジスタの電流能力に従った基準電流がドレインーソース間に流れる電圧となり、その後前記第２及び第３のスイッチがオフ状態となると、前記容量素子に前記トランジスタのゲートーソース間電圧が保持され、この保持されたゲートーソース間電圧に基づく基準電流を出力するか否かが前記第１のスイッチの動作により決定されることを特徴とする請求項７乃至９のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項１１】　前記第３のスイッチは、前記第２のスイッチがオフ状態になった後にオフ状態になることを特徴とする請求項１０に記載の電流負荷デバイス駆動用半導体装置。

【請求項１２】　前記第１乃至３のスイッチがトランジスタから構成されていることを特徴とする請求項７乃至１１のいずれか１項に記載の電流負荷デバイス駆動用半

導体装置。

【請求項１３】　前記１ビットデジタル／電流変換回路は、前記第２のスイッチを構成するトランジスタのゲートに入力する信号の反転信号がゲートに入力され、ゲートの長さと幅との積が前記第２のスイッチを構成するトランジスタのゲートの長さと幅との積の１／２であり、ドレインが前記第１のトランジスタのゲートに接続されソースがドレインに短絡されたダミートランジスタを有することを特徴とする請求項１２に記載の電流負荷デバイス駆動用半導体装置。

【請求項１４】　前記ｎビットデジタル／電流変換回路は、入力される１種の前記基準電流よりｎ以下の複数の電流値を記憶し、記憶した電流値数と同数ビットのデジタルデータにより前記複数の記憶電流を出力するか否かを決めるデジタル／電流変換回路の記憶した電流値数がｎになるように、前記デジタル／電流変換回路を１又は複数個備えることを特徴とする請求項１乃至３いずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項１５】　前記デジタル／電流変換回路は、１種の基準電流より記憶する複数の電流値の内、１つが前記入力される基準電流値であることを特徴とする請求項１４に記載の電流負荷デバイス駆動用半導体装置。

【請求項１６】　１又は複数の前記デジタル／電流変換回路により構成される前記ｎビットデジタル／電流変換回路のそれぞれの出力電流値の比は、最も低い電流値から順次２倍したものに設定されており、出力を並列に接続したものを前記ｎビットデジタル／電流変換回路の出力とすることで、ｎビットデジタルデータに従って、２ｎレベルの電流値を出力することができることを特徴とする請求項１４又は１５に記載の電流負荷デバイス駆動用半導体装置。

【請求項１７】　前記デジタル／電流変換回路は、前記基準電流が流れる信号線と、夫々に前記デジタル画像データの１ビットが伝達されるｋ（ｋはｎ以下の自然数）本のデータ線と、制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された電流記憶用トランジスタと、互いにゲートが短絡されソースが第１の電圧供給線に共通接続されたｋ個の電流出力用トランジスタと、前記電流出力用トランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、夫々前記ｋ個の電流出力用トランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号のいずれかにより制御されるｋ個の出力制御用スイッチと、前記電流記憶用トランジスタのドレインと前記信号線との間に接続され前記制御線を伝達する信号により制御される第１の記憶制御用スイッチと、前記電流記憶用トランジスタのゲートと前記電流出力用トランジスタのゲートとの間に接続され前記制御線を伝達する信号により制御される第２の記憶制御用スイッチと、を備えていることを特徴とする請求項１４乃至１６のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項１８】　前記デジタル／電流変換回路は、前記基準電流が流れる信号線と、夫々に前記デジタル画像データの１ビットが伝達されるｋ本のデータ線と、第１及び第２の制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された電流記憶用トランジスタと、互いにゲートが短絡されソースが第１の電圧供給線に共通接続されたｋ個の電流出力用トランジスタと、前記電流出力用トランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、夫々前記ｋ個の電流出力用トランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号のいずれかにより制御されるｋ個の出力制御用スイッチと、前記電流記憶用トランジスタのドレインと前記信号線との間に接続され前記第２の制御線を伝達する信号により制御される第１の記憶制御用スイッチと、前記電流記憶用トランジスタのゲートと前記電流出力用トランジスタのゲートとの間に接続され前記第１の制御線を伝達する信号により制御される第２の記憶制御用スイッチと、を備えていることを特徴とする請求項１４乃至１６のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項１９】　前記デジタル／電流変換回路は、前記基準電流が流れる信号線と、夫々に前記デジタル画像データの１ビットが伝達されるｋ本のデータ線と、制御線と、第１及び第２の電圧供給線と、電流記憶かつ出力用トランジスタと、ゲートが前記電流記憶かつ出力用トランジスタのゲートと短絡されソースがｋ－１個の電流出力用トランジスタと、前記電流出力用トランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、夫々前記電流記憶かつ出力用トランジスタとｋ－１個の電流出力用トランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号のいずれかにより制御されるｋ個の出力制御用スイッチと、前記電流記憶かつ出力用トランジスタのドレインと前記信号線との間に接続され前記制御線を伝達する信号により制御される第１の記憶制御用スイッチと、前記電流記憶かつ出力用トランジスタのゲートと前記電流記憶かつ出力用トランジスタのドレイン又は信号線との間に接続され前記制御線を伝達する信号により制御される第２の記憶制御用スイッチと、を備えていることを特徴とする請求項１４乃至１６のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項２０】　前記デジタル／電流変換回路は、前記基準電流が流れる信号線と、夫々に前記デジタル画像データの１ビットが伝達されるｋ本のデータ線と、第１及び第２の制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された電流記憶かつ出力用トランジスタと、ゲートが前記電流記憶かつ出力用トランジスタのゲートと短絡されソースが第１の電圧供給線に共通接続されたｋ－１個の電流出力用トランジス

タと、前記電流出力用トランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、夫々前記電流記憶かつ出力用トランジスタとｋ－１個の電流出力用トランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号のいずれかにより制御されるｋ個の出力制御用スイッチと、前記電流記憶かつ出力用トランジスタのドレインと前記信号線との間に接続され前記第２の制御線を伝達する信号により制御される第１の記憶制御用スイッチと、前記電流記憶かつ出力用トランジスタのゲートと前記電流記憶かつ出力用トランジスタのドレイン又は信号線との間に接続され前記第１の制御線を伝達する信号により制御される第２の記憶制御用スイッチと、を備えていることを特徴とする請求項１４乃至１６のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項２１】　前記電流記憶用又は電流記憶かつ出力用トランジスタと、前記出力用トランジスタのそれぞれのソースと前記第１の電圧供給線の間に、ゲートが第３の電圧供給線によりバイアスされている複数の第２のトランジスタを追加された前記１ビットデジタル／電流変換回路を備えることを特徴とする請求項１７乃至２０のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項２２】　前記電流記憶かつ出力用トランジスタの電流能力は、前記電流出力用トランジスタにおける最も電流能力が高いトランジスタと同じかそれ以上であることを特徴とする請求項１７乃至２１のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項２３】　前記出力制御用スイッチがオフの状態で前記第１及び第２の記憶制御用スイッチがオン状態のときに、前記電流記憶用トランジスタは、そのゲートードレイン間が短絡されて飽和領域で動作し、その動作が安定した段階における前記電流記憶用トランジスタのゲートーソース間電圧は、前記基準電流をドレインーソース間に流すために必要な電圧となり、その値は前記電流記憶用トランジスタの電流能力に従い決定され、その後前記第１及び第２の記憶制御用スイッチがオフ状態になると、前記容量素子に前記電流記憶用トランジスタのゲートーソース間電圧が保持され、この保持されたゲートーソース間電圧に基づく基準電流から前記ｎ個の電流出力用トランジスタが夫々の電流能力に基づいた総計でｎ種の電流を流すことができる状態となり、前記電流出力用トランジスタが流すことができる電流を出力するか否かが前記ｎビットのデジタル画像データによって決定されることを特徴とする請求項１７乃至２２のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項２４】　前記第２の記憶制御用スイッチは、前記第１の記憶制御用スイッチがオフ状態になった後にオフ状態になることを特徴とする請求項２３に記載の電流負荷デバイス駆動用半導体装置。

【請求項２５】　前記出力制御用スイッチ並びに第１及び第２の記憶制御用スイッチがトランジスタから構成されていることを特徴とする請求項１４乃至２４のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項２６】　前記デジタル／電流変換回路は、前記第２の制御線を伝達する信号の反転信号がゲートに入力されゲートの長さと幅との積が前記第１の記憶制御用スイッチを構成するトランジスタのゲートの長さと幅との積の１／２でありドレインが前記電流記憶用トランジスタのゲートに接続されソースがドレインに短絡されたダミートランジスタを有することを特徴とする請求項２５に記載の電流負荷デバイス駆動用半導体装置。

【請求項２７】　前記ｎビットデジタル／電流変換回路は、請求項７乃至１３のいずれかに記載のｐビットデジタル／電流変換回路と、請求項１７乃至２６のいずれかに記載のｍビットデジタル／電流変換回路とを（ｐ、ｍは自然数。ｐ＋ｍ＝ｎ）組み合わせることにより構成されていることを特徴とする電流負荷デバイス駆動用半導体装置。

【請求項２８】　前記第１及び第２の電源線が共通の電源線とされていることを特徴とする請求項７乃至１３、及び１７乃至２７のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項２９】　前記ｎビットデジタル／電流変換回路の数がａ、前記電流負荷デバイス内の電流負荷素子の電流と動作の関係が異なる種類がｂであり、１又は複数種の前記基準電流は、ｂ種の電流負荷素子にそれぞれ対応するものが準備されており、前記基準電流値を記憶する電流記憶動作がａ／ｂ回に分けて行われることを特徴とする請求項１乃至２８のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項３０】　前記ｎビットデジタル／電流変換回路の数がａである群が２つ以上あり、前記電流負荷デバイス内の電流負荷素子の電流と動作の関係が異なる種類がｂであり、任意のフレームにおいて、ある群を電流出力用回路とし、他の群のいずれかを電流記憶用回路とし、電流の記憶は各フレーム内で同じ基準電流を用いてａ／ｂ回に分けて行われ、フレーム毎又は数フレーム毎に電流出力と電流記憶との役割を変更することを特徴とする請求項１乃至２８のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項３１】　前記記憶動作は、前記電流負荷デバイス駆動用半導体装置内にあるシフト数がａ／ｂビット以上のシフトレジスタの出力信号に同期して行われることを特徴とする請求項１乃至３０いずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項３２】　電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、複数の電流出力回路と、プリチャージ回路と、を有し、前記プリチャージ回路は、前記電流負荷デバイス内のデータ

線を経由して、前記データ線上のセルに、前記電流出力回路の出力電流により決まる電圧を供給すること、及び前記電流出力回路の出力電流をそのまま供給することが可能であることを特徴とする電流負荷デバイス駆動用半導体装置。

【請求項３３】　前記プリチャージ回路は、前記電流出力回路からの出力電流により駆動される電流負荷デバイス内の負荷と同等な負荷である擬似負荷回路と、前記疑似負荷に前記電流出力回路の出力電流が供給された際に生じる電圧をインピーダンス変換して出力するボルテージフォロワと、を有することを特徴とする請求項３２に記載の電流負荷デバイス駆動用半導体装置。

【請求項３４】　前記プリチャージ回路の擬似負荷回路は、電流負荷素子と同等な負荷、あるいは、電流を保持・供給するセル回路負荷と同等な回路負荷とすることを特徴とする請求項３３に記載の電流負荷デバイス駆動用半導体装置。

【請求項３５】　１水平期間の初期にプリチャージ動作として前記擬似負荷回路に前記電流出力回路の出力電流を供給して得られた電圧を、前記プリチャージ回路内のボルテージフォロワによってインピーダンス変換し、前記電流負荷デバイスのデータ線を経由して、前記電流負荷デバイス内のセル内の電流負荷素子又はセル回路負荷に印加し、その後電流駆動動作として、前記電流出力回路の出力電流を、前記電流負荷デバイスのデータ線を経由して、直接前記電流負荷デバイス内のセル内の電流負荷素子又はセル回路負荷に供給することを特徴とする請求項３３又は３４に記載の電流負荷デバイス駆動用半導体装置。

【請求項３６】　前記プリチャージ回路は、前記ボルテージフォロワのオフセット電圧をキャンセルする構成を有することを特徴とする請求項３３乃至３５のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項３７】　前記プリチャージ回路内のボルテージフォロワのオフセット電圧をキャンセルする動作は、１又は数フレームに一度行うことを特徴とする請求項３６に記載の電流負荷デバイス駆動用半導体装置。

【請求項３８】　前記電流出力回路は、請求項１乃至３１のいずれかに記載のｎビットデジタル／電流変換回路であることを特徴とする請求項３２乃至３７のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項３９】　電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、１つ又は複数の基準電流値を記憶し、ｎビットデジタルデータに従って電流を出力する複数のｎビットデジタル／電流変換回路と、順々に行われる前記ｎビットデジタル／電流変換回路の前記基準電流の記憶動作と同期する走査信号を出力する電流記憶用シフトレジスタと、ｎビットデジタルデータをｎビットデータセレクタに伝えるｎビットデータラッチと、前記ｎビットデジタル／電流変換回路が前記基準電流を記憶する動作を行うか、電流を出力する動作を行うかにより、前記ｎビットデータラッチからのｎビットデジタルデータをｎビットデジタル／電流変換回路に伝えるか否かを決めるｎビットデータセレクタと、を少なくとも備えることを特徴とする電流負荷デバイス駆動用半導体装置。

【請求項４０】　電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、前記基準電流を生成する回路を備えることを特徴とする請求項３９に記載の電流負荷デバイス駆動用半導体装置。

【請求項４１】　前記ｎビットデジタル／電流変換回路が請求項１乃至３１のいずれかに記載のｎビットデジタル／電流変換回路であることを特徴とする請求項４０に記載の電流負荷デバイス駆動用半導体装置。

【請求項４２】　電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、電流を出力する前に電圧を出力するプリチャージ動作を行うプリチャージ回路を備えることを特徴とする請求項３９乃至４１のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項４３】　前記プリチャージ回路が請求項３２乃至３８のいずれか１項に記載のプリチャージ回路であることを特徴とする請求項４２に記載の電流負荷デバイス駆動用半導体装置。

【請求項４４】　電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、入力されるｎビットデジタルデータを保持する動作と前記データラッチに出力するｎビットデータレジスタと、順々に行われる前記ｎビットデータレジスタのｎビットデジタルデータの保持動作と同期する信号を出力するデータ保持用シフトレジスタと、を少なくとも備えることを特徴とする請求項３９乃至４３いずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項４５】　電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、前記電流出力回路やプリチャージ回路の出力と、電流負荷デバイスの複数のデータ線のいずれか１つを接続する出力セレクタを備えることを特徴とする請求項３９乃至４４のいずれか１項に記載の電流負荷デバイス駆動用半導体装置。

【請求項４６】　電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、前記出力セレクタにより、１水平期間において、複数のデータ線を順々に選択し駆動することで、データ線数よりも少ない前記電流出力回路やプリチャージ回路数により電流負荷デバイスを駆動することを特徴とする請求項４５に記載の電流負荷デバイス駆動用半導体装置。

【請求項４７】　全てのトランジスタが薄膜トランジスタとして１つのチップに集積された請求項１乃至４６のいずれか１項に記載の電流負荷デバイス駆動用半導体装

置。
【請求項４８】　前記電流負荷素子が発光素子である請求項１乃至４７のいずれか１項に記載の発光表示装置駆動用半導体装置。
【請求項４９】　前記電流負荷素子が有機ＥＬ素子である請求項１乃至４７のいずれか１項に記載の有機ＥＬ表示装置駆動用半導体装置。
【請求項５０】　電流負荷素子と同一基板上に請求項１乃至４９のいずれか１項に記載の電流負荷デバイス駆動用半導体装置が作成された電流負荷デバイス。
【請求項５１】　各前記電流負荷セル内の前記電流負荷素子又は前記電流を保持・供給するセル回路と同一な構成・サイズを持つ負荷を前記プリチャージ回路内の疑似負荷として備えることを特徴とする電流負荷デバイス駆動用半導体装置を備えた請求項５０に記載の電流負荷デバイス。
【請求項５２】　前記電流負荷素子が発光素子であることを特徴とする電流負荷デバイス駆動用半導体装置を備えた請求項５０又は５１に記載の電流負荷デバイス。
【請求項５３】　前記電流負荷素子が有機ＥＬ素子であることを特徴とする電流負荷デバイス駆動用半導体装置を備えた請求項５０又は５１に記載の電流負荷デバイス。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、電流負荷素子を含んだセルを複数備える電流負荷デバイスを駆動するための電流負荷デバイス駆動用半導体装置及びそれを備えた電流負荷デバイスに関し、特に電流負荷素子が供給される電流値により階調表示を行う電流負荷デバイス駆動用半導体装置及びそれを備えた電流負荷デバイスに関する。
【０００２】
【従来の技術】供給される電流により動作が決定される電流負荷素子含んだセルをマトリックス状に複数備える電流負荷デバイスが開発されている。その応用は、例えば、電流負荷素子が発光素子である発光表示装置であり、また、発光素子として有機ＥＬ素子が用いられている有機ＥＬ表示装置である。
【０００３】以下、電流負荷デバイスとして、発光表示装置を例にとって説明する。図３５はマトリックス型発光表示装置の構成を示す。
【０００４】表示装置は、水平駆動回路２００、垂直走査（駆動）回路３００及び表示部４００から構成される。階調表示は、表示部４００の１画素表示部１００内にある発光素子に流れる電流を調節することで実現される。多種の電流により輝度が決定される発光素子では、電流と輝度とは比例関係にある。また、１画素表示部１００の構成と水平駆動回路２００及び垂直走査回路３００から印加される電流又は電圧との組み合わせによって、発光表示装置の駆動方法は単純マトリックス駆動とアクティブマトリックス駆動とに分類される。
【０００５】図３６は単純マトリックス駆動の場合の１画素表示部の構成を示す回路図である。単純マトリックス駆動の場合の１画素表示部１０１では、制御線１１０と信号線１２０との各交点において、発光素子１３０が制御線１１０と信号線１２０との間に接続されている。図３５に示すように、制御線１１０は垂直走査回路３００により駆動され、信号線１２０は水平駆動回路２００により駆動される。
【０００６】そして、垂直走査回路３００により制御線１１０が１本毎に順次選択され、第Ｋ番目の制御線１１０を走査している期間に、水平駆動回路２００から第Ｌ番目の信号線１２０に電流又は電圧が出力されると、第Ｋ行第Ｌ列目の発光素子に流れる電流が決定され、その発光素子がその電流に対応する強度で発光する。その後、第（Ｋ＋１）番目の走査が開始されると、第Ｋ行目の発光素子の発光は終了する。
【０００７】図３７はアクティブマトリックス駆動の場合の１画素表示部の構成を示す回路図である。アクティブマトリックス駆動の場合の１画素表示部１０２では、制御線１１０と信号線１２０との各交点において、制御線１１０の電位により制御されるスイッチＳＷ１００が信号線１１０に接続され、スイッチＳＷ１００の他端にＴＦＴ（Thin Film Transistor：薄膜トランジスタ）Ｔ１００のゲート及び容量素子Ｃ１００の一端が接続されている。ＴＦＴ１００のソース及び容量素子Ｃ１００の他端は接地され、ＴＦＴ１００のドレインと電位がＶＥＬの信号線との間に発光素子１３０が接続されている。
【０００８】そして、垂直走査回路３００により制御線１１０が１本毎に順次選択され、第Ｋ番目の制御線１１０が選択されると、１画素表示部１０２内のスイッチＳＷ１００がオンとなる。このときに水平駆動回路２００の第Ｌ番目の出力電圧がＴＦＴ１００のゲート電圧となり、ＴＦＴ１００が飽和領域で動作するようなゲート電圧が印加されると、ＴＦＴ１００のインピーダンスが決定される。この結果、発光素子１３０に流れる電流が決定され、発光素子１３０がその電流に対応する強度で発光する。
【０００９】アクティブマトリックス駆動の場合には、１画素表示部は他の構成をとることもある。図３８（ａ）及び図３８（ｂ）はアクティブマトリックス駆動の場合の１画素表示部の他の構成を示す回路図である。図３８（ａ）に示すように、他の構成の１画素表示部１０３では、制御線１１０の電位により制御されるスイッチＳＷ１０２が信号線１１０に接続され、スイッチＳＷ１０２の他端にＰチャネルＴＦＴ１０２のゲート及びドレインが接続されている。このゲート及びドレインには、制御線１１０の電位により制御されるスイッチＳＷ

１０１が接続され、その他端にＰチャネルＴＦＴＴ１０１のゲート及び容量素子Ｃ１００の一端が接続されている。ＴＦＴＴ１０１及びＴ１０２のソース及び容量素子Ｃ１００の他端には、定電位ＶＥＬが供給される。ＴＦＴＴ１０１のドレインと接地電位ＧＮＤとの間に発光素子１３０が接続されている。

【００１０】そして、垂直走査回路３００により第Ｋ番目の制御線１１０が選択され、スイッチＳＷ１０１及びＳＷ１０２がオンとなると、水平駆動回路２００の第Ｌ番目の出力電流を信号線１２０から流すように、ＴＦＴＴ１０２のゲート電圧が決まる。ＴＦＴＴ１０２及びＴＦＴＴ１０１はカレントミラー構成を採っているため、ＴＦＴＴ１０２及びＴＦＴＴ１０１の電流能力が互いに等しい場合には、ＴＦＴＴ１０１を通して、発光素子１３０に水平駆動回路２００の出力電流値と同じ電流が流れ、発光素子１３０がその電流値に応じた強度で発光する。

【００１１】図３８（ｂ）に示すように、ＰチャネルＴＦＴＴ１０１及びＴ１０２の代わりにＮチャネルＴＦＴＴ１０３及びＴ１０４を使用した場合にも、同様の動作が行われる。

【００１２】単純マトリックス駆動とアクティブマトリックス駆動とを比べると、アクティブマトリックス駆動の場合には、次の行が選択された後でも電圧が容量素子に蓄積されているため、電流を流し続けることができる。従って、瞬間的に発光するのみの単純マトリックス駆動の場合に比べ、発光素子に流す電流は小さくなる。

【００１３】このように、電流又は電圧の絶対値が異なったとしても、単純マトリックス駆動及びアクティブマトリックス駆動の駆動方法の種類に関わらず、階調表示を行う場合には、水平駆動回路２００はデジタル階調データを電流又は電圧に変換する機能を有する。しかし、電圧出力であると、画素回路（１画素表示部）内にトランジスタのしきい値のばらつき並びに発光素子の電圧－電流特性及び電流－輝度特性のばらつきが存在するため、同じ電圧を印加しても輝度がばらつく可能性が高い。一方、電流出力の場合には、発光素子の電流－輝度特性のばらつきのみの影響を受けるので、輝度のばらつきは小さく、精度の高い表示が可能となる。

【００１４】図３９は表示部４００に電流を出力するための水平駆動回路２００の構成の一例を示すブロック図である。この構成では、デジタル階調データをデータロジック部２０１にて出力数分に展開した後、それらのデジタル階調データを、デジタル／電流変換部２１０に入力することで、出力数分の電流出力を得る。

【００１５】図４０は１出力分のデジタル／電流変換部の第１の従来例を示す回路図である。階調データが３ビット（Ｄ０乃至Ｄ２）の場合、夫々これらにより制御されるスイッチＳＷ１１０、ＳＷ１１１、ＳＷ１１２が電流Ｉｄａｔａを出力する出力端に共通接続されている。スイッチＳＷ１１０、ＳＷ１１１、ＳＷ１１２と接地電位ＶＧにある接地線との間に、夫々ゲートに入力電圧ＶＡが供給されるＮチャネルＴＦＴＴ１１０、Ｔ１１１、Ｔ１１２が接続されている。なお、発光素子の電流－輝度特性は比例関係にあるものとする。また、水平駆動回路２００、垂直走査回路３００を共にガラス基板上に形成する場合を想定しており、トランジスタはすべてＴＦＴとなっている。なお、階調データが３ビット以上の場合でも同様に構成される。

【００１６】また、第１の従来例では、ＴＦＴＴ１１０、Ｔ１１１及びＴ１１２について、各チャネル長（Ｌ）が一定となり、チャネル幅（Ｗ）の比が１：２：４となるように設計されている。ＴＦＴＴ１１０乃至Ｔ１１２においては、ゲート電圧が電圧ＶＡ、ソース電圧が電圧ＶＧといずれも共通になっているので、ＴＦＴＴ１１０乃至ＴＴ１１２が飽和領域で動作している場合には、電流比が１：２：４となる。よって、適当な入力電圧ＶＡを選択すれば、階調データＤ０乃至Ｄ２に基づいてスイッチＳＷ１１０乃至ＳＷ１１２をオン／オフすることで、出力電流Ｉｄａｔａについて、電流比が０～７となる８階調の電流出力が可能となる。また、電流の絶対値は、入力電圧ＶＡを変更することで調整することができる。

【００１７】図４１は１出力分のデジタル／電流変換部の第２の従来例を示す回路図である。第２の従来例では、ＮチャネルＴＦＴＴ１１０乃至Ｔ１１２のゲートにデジタル階調データＤ０乃至Ｄ２が入力される。ＴＦＴＴ１１０乃至Ｔ１１２のドレインは出力端に共通接続され、ソースには電源電圧ＶＤが供給される。なお、ＴＦＴＴ１１０乃至Ｔ１１２のチャネル幅の比は、第１の従来例と同様に、１：２：４に設定されている。

【００１８】このような第２の従来例では、スイッチを設ける代わりに、デジタル階調データ入力のハイレベルを予め適当な電圧に設定しておき、ロウレベルを薄膜トランジスタがオフするレベルとすることで、第１の従来例と同様に、電流比が０～７となる８階調の電流出力が可能となる。また、電流の絶対値は、デジタル階調データ入力のハイレベルを変更することで調整することができる。

【００１９】

【発明が解決しようとする課題】しかしながら、トランジスタ、特にＴＦＴでは、異なるＴＦＴ間で同じゲート電圧が印加された場合の電流能力のばらつきが大きいため、精度の高い電流出力を出すことが難しいという問題点がある。従来のデジタル／電流変換部では、ほぼ電流負荷デバイス幅全域にてＴＦＴの特性ばらつきがあると、ＴＦＴのサイズが均一で、かつゲート－ソース間電圧が均一であっても、ばらついた部分では電流値が他の領域と異なるために、表示むらが発生してしまう。また、近接領域にあるようなＴＦＴ間でも電流能力がばら

つき、そのばらつきが大きくなると、隣接画素との間で表示むらが発生したり、同じ出力に使用されるＴＦＴの特性がばらつくと階調の単調性も満足しなくなったりする。

【００２０】また、従来のデジタル／電流変換部では、特にアクティブマトリックス駆動において、出力電流値が低い場合に、駆動に時間がかかるという問題点もある。これは、電流駆動によるアクティブマトリックス駆動を採用すると、画素内のＴＦＴに、駆動回路であるデジタル／電流変換部の出力電流と同じ電流が流れた時点で駆動が完了するのであるが、表示部４００内の信号線１１０には、必ず配線負荷、特に寄生容量が存在し、発光素子も容量値を持つため、一定電流である出力電流でそれらの容量負荷を充放電する必要があるためである。つまり、それらの容量をある電圧に充放電してはじめて、画素内のＴＦＴに駆動回路であるデジタル／電流変換回路の出力電流と同じ電流が流れるため、それまでに長い時間がかかる。

【００２１】本発明はかかる問題点に鑑みてなされたものであって、入力されるデジタル画像データに対し、精度の高い出力電流を供給することができ、好ましくは出力電流値が低い場合でも高速で発光表示装置を駆動することができる発光表示装置駆動用半導体装置及びそれを備えた発光表示装置を提供し、更に一般的な電流負荷デバイス駆動用半導体装置及びそれを備えた電流負荷デバイスを提供することを目的とする。

【００２２】

【課題を解決するための手段】本発明に係る電流負荷デバイス駆動用半導体装置は、電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、入力される１種又は複数種の基準電流により決定されるｎ（ｎは自然数）種の電流値を記憶する機能と、前記記憶電流値から得られる２ｎレベルの電流値の内、入力されるｎビットデジタルデータに従って１つの電流を出力する機能を備えるｎビットデジタル／電流変換回路を、１つ又は複数の前記セルへの供給端子毎に少なくとも一つ備えることを特徴とする。

【００２３】本発明に係る他の電流負荷デバイス駆動用半導体装置は、電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、複数の電流出力回路と、プリチャージ回路と、を有し、前記プリチャージ回路は、前記電流負荷デバイス内のデータ線を経由して、前記データ線上のセルに、前記電流出力回路の出力電流により決まる電圧を供給すること、及び前記電流出力回路の出力電流をそのまま供給することが可能であることを特徴とする。

【００２４】本発明に係る更に他の電流負荷デバイス駆動用半導体装置は、電流負荷素子を含んだセルを複数備える電流負荷デバイスの駆動用半導体装置において、１つ又は複数の基準電流値を記憶し、ｎビットデジタルデータに従って電流を出力する複数のｎビットデジタル／電流変換回路と、順々に行われる前記ｎビットデジタル／電流変換回路の前記基準電流の記憶動作と同期する走査信号を出力する電流記憶用シフトレジスタと、ｎビットデジタルデータをｎビットデータセレクタに伝えるｎビットデータラッチと、前記ｎビットデジタル／電流変換回路が前記基準電流を記憶する動作を行うか、電流を出力する動作を行うかにより、前記ｎビットデータラッチからのｎビットデジタルデータをｎビットデジタル／電流変換回路に伝えるか否かを決めるｎビットデータセレクタと、を少なくとも備えることを特徴とする。

【００２５】そして、本発明を、発光表示装置駆動用半導体装置又は発光表示装置に適用したときの構成は、以下のとおりである。

【００２６】即ち、本発明に係る第１の発光表示装置駆動用半導体装置は、供給される電流によって輝度が決まる発光素子が各画素に設けられた発光表示装置を駆動する発光表示装置駆動用半導体装置において、１ビット分の基準電流値を記憶するｎ個の１ビットデジタル／電流変換回路を備え夫々が１個の前記１ビットデジタル／電流変換回路に記憶される前記発光素子の電流－輝度特性に対応したｎ種の基準電流を入力しｎビットのデジタル画像データに基づいて選択した１又は２以上の１ビットデジタル／電流変換回路に前記基準電流を出力させることにより２ｎ種の電流を出力するｎビットデジタル／電流変換回路を前記発光表示装置に電流を出力する出力端子毎に有し、前記ｎ種の基準電流の電流値は、夫々最も低い電流値に対して順次２倍したものに設定されていることを特徴とする。

【００２７】なお、前記１ビットデジタル／電流変換回路は、前記基準電流が流れる信号線と、前記デジタル画像データの１ビットが伝達されるデータ線と、制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された第１のトランジスタと、前記第１のトランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、前記第１のトランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号により制御される第１のスイッチと、前記第１のトランジスタのゲートと前記信号線又は前記第１のトランジスタのドレインとの間に接続され前記制御線を伝達する信号により制御される第２のスイッチと、前記第１のトランジスタのドレインと前記信号線との間に接続され前記制御線を伝達する信号により制御される第３のスイッチと、を有してもよく、前記基準電流が流れる信号線と、前記デジタル画像データの１ビットが伝達されるデータ線と、第１及び第２の制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された第１のトランジスタと、前記第１のトランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、前記第１のトランジスタのドレインと

前記出力端子との間に接続され前記データ線を伝達する信号により制御される第１のスイッチと、前記第１のトランジスタのゲートと前記信号線又は前記第１のトランジスタのドレインとの間に接続され前記第２の制御線を伝達する信号により制御される第２のスイッチと、前記第１のトランジスタのドレインと前記信号線との間に接続され前記第１の制御線を伝達する信号により制御される第３のスイッチと、を有してもよい。

【００２８】又は、前記第１のトランジスタと前記第１の電圧供給線との間に、ゲートがバイアスされた第２のトランジスタを有しても良い。

【００２９】また、前記第１のスイッチがオフ状態で前記第２及び第３のスイッチがオン状態のときに、前記トランジスタは、そのゲートードレイン間が短絡されて飽和領域で動作し、その動作が安定した段階における前記トランジスタのゲートーソース間電圧は、前記基準電流をドレインーソース間に流すために必要な電圧となり、その値は前記トランジスタの電流能力に従い決定され、その後前記第２及び第３のスイッチがオフ状態となると、前記容量素子に前記トランジスタのゲートーソース間電圧が保持され、この保持されたゲートーソース間電圧に基づく基準電流を出力するか否かが前記第１のスイッチの動作により決定されれば、各出力にｎ個の前記１ビットデジタル／電流変換回路があるため、前記ｎビットデジタル画像データに従い、前記発光素子の電流ー輝度特性に従う２ｎレベルの電流が出力できる。従って、前記１ビットデジタル／電流変換回路は、前記電流を記憶・出力するトランジスタの電流能力ばらつきに関わらず、高い精度の電流を出力することができる。

【００３０】更に、前記第３のスイッチは、前記第２のスイッチがオフ状態になった後にオフ状態になれば、前記第３のスイッチとしてのトランジスタのオフ動作によるノイズの影響が小さくなるため、前記１ビットデジタル／電流変換回路は、より高精度に電流を記憶・出力することができる。

【００３１】前記第１乃至第３のスイッチがトランジスタから構成されていてもよい。

【００３２】また、前記１ビットデジタル／電流変換回路に、前記第２の制御線を伝達する信号の反転信号がゲートに入力されゲートの長さと幅との積が前記第２のスイッチを構成するトランジスタのゲートの長さと幅との積の１／２でありドレインが前記トランジスタのゲートに接続されソースがドレインに短絡されたダミートランジスタを設けることにより、前記第２のスイッチとしてのトランジスタがオフする際の電荷の移動を補償できるため、前記１ビットデジタル／電流変換回路は、より高精度に電流を記憶・出力することができる。

【００３３】本発明においては、電流記憶期間において、各ｎビットデジタル／電流変換回路にあるｎ個の電流を記憶する第１のトランジスタは、ゲートードレイン間を短絡して飽和領域で動作しており、ゲートーソース間電圧は、基準電流が安定して流れる電圧となっている。電流記憶期間の終了時に、ゲートードレイン間を短絡しているスイッチをオフし、前記ゲートーソース間電圧を容量に保存する。この時、前記ｎ個の第１のトランジスタは、それぞれの電流能力に従い、基準電流を流すゲートーソース間電圧を記憶するため、前記ｎ個の第１のトランジスタの電流能力ばらつきに関わらず、基準電流を流すようなゲートーソース間電圧を保持することで、電流を記憶する。駆動期間において、前記ｎ個の電流を記憶した第１のトランジスタは、画像デジタルデータに従い、前記ｎ個の電流を記憶した第１のトランジスタの夫々のドレインと前記デジタル／電流変換回路の出力との間にあるｎ個のスイッチをオン／オフすることで、記憶した電流を出力するか否かを決める。このように出力された電流は、前記ｎ個の電流を記憶したトランジスタ自身より出力されるため、電流能力ばらつきの影響のない、精度の高いものとなる。以上のような動作により、本発明のｎビットデジタル／電流変換回路は、電流比が０、１、２、・・・、２ｎ－１となる精度の高い電流を出力することが可能となる。この場合、ｎビットデジタル／電流変換回路を構成するためには、ｎ個の基準電流源が必要となる。

【００３４】また、前記ゲートがバイアスされた第２のトランジスタを有する際には、前記第１のトランジスタと第２のトランジスタは、カスコード接続されており、共に飽和領域で動作する場合、ドレイン電流のドレイン電圧依存性を抑えることができるため、発光素子の特性がばらついても、供給される電流のばらつきを抑えることができる。

【００３５】本発明に係る第２の発光表示装置駆動用半導体装置は、供給される電流によって輝度が決まる発光素子が各画素に設けられた発光表示装置を駆動する発光表示装置駆動用半導体装置において、１種の基準電流値を記憶しｎビットのデジタル画像データに基づいて前記記憶された基準電流から前記発光素子の電流ー輝度特性に対応した２ｎ種の電流を生成して出力するｎビットデジタル／電流変換回路を前記発光表示装置に電流を出力する出力端子毎に有することを特徴とする。

【００３６】なお、前記ｎビットデジタル／電流変換回路は、前記基準電流が流れる信号線と、夫々に前記デジタル画像データの１ビットが伝達されるｎ本のデータ線と、制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された電流記憶用トランジスタと、互いにゲートが短絡されソースが第１の電圧供給線に共通接続されたｎ個の電流出力用トランジスタと、前記電流出力用トランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、夫々前記ｎ個の電流出力用トランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号のいずれ

かにより制御されるｎ個の出力制御用スイッチと、前記電流記憶用トランジスタのドレインと前記信号線との間に接続され前記制御線を伝達する信号により制御される第１の記憶制御用スイッチと、前記電流記憶用トランジスタのゲートと前記電流出力用トランジスタのゲートとの間に接続され前記制御線を伝達する信号により制御される第２の記憶制御用スイッチと、を有し、前記ｎ個の電流出力用トランジスタの電流能力は、夫々最も低い電流能力に対して順次２倍したものに設定されていてもよく、ｎビットデジタル／電流変換回路は、前記基準電流が流れる信号線と、夫々に前記デジタル画像データの１ビットが伝達されるｎ本のデータ線と、第１及び第２の制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続された電流記憶用トランジスタと、互いにゲートが短絡されソースが第１の電圧供給線に共通接続されたｎ個の電流出力用トランジスタと、前記電流出力用トランジスタのゲートと前記第２の電圧供給線との間に接続された容量素子と、夫々前記ｎ個の電流出力用トランジスタのドレインと前記出力端子との間に接続され前記データ線を伝達する信号のいずれかにより制御されるｎ個の出力制御用スイッチと、前記電流記憶用トランジスタのドレインと前記信号線との間に接続され前記第２の制御線を伝達する信号により制御される第１の記憶制御用スイッチと、前記電流記憶用トランジスタのゲートと前記電流出力用トランジスタのゲートとの間に接続され前記第１の制御線を伝達する信号により制御される第２の記憶制御用スイッチと、を有し、前記ｎ個の電流出力用トランジスタの電流能力は、夫々最も低い電流能力に対して順次２倍したものに設定されていてもよい。

【００３７】又は、前記電流記憶用トランジスタや前記電流出力用トランジスタと前記第１の電圧供給線との間に、夫々、ゲートがバイアスされたバイアストランジスタを有しても良い。

【００３８】また、前記出力制御用スイッチがオフの状態で前記第１及び第２の記憶制御用スイッチがオン状態のときに、前記電流記憶用トランジスタは、そのゲートードレイン間が短絡されて飽和領域で動作し、その動作が安定した段階における前記電流記憶用トランジスタのゲートーソース間電圧は、前記基準電流をドレインーソース間に流すために必要な電圧となり、その値は前記電流記憶用トランジスタの電流能力に従い決定され、その後前記第１及び第２の記憶制御用スイッチがオフ状態になると、前記容量素子に前記電流記憶用トランジスタのゲートーソース間電圧が保持され、この保持されたゲートーソース間電圧に基づく基準電流から前記ｎ個の電流出力用トランジスタが夫々の電流能力に基づいた総計でｎ種の電流を流すことができる状態となり、前記電流出力用トランジスタが流すことができる電流を出力するか否かが前記ｎビットのデジタル画像データによって決定されてもよい。

【００３９】更に、前記第２の記憶制御用スイッチは、前記第１の記憶制御用スイッチがオフ状態になった後にオフ状態になることが好ましい。

【００４０】前記出力制御用スイッチ並びに第１及び第２の記憶制御用スイッチがトランジスタから構成されていてもよい。

【００４１】また、前記ｎビットデジタル／電流変換回路は、前記第２の制御線を伝達する信号の反転信号がゲートに入力されゲートの長さと幅との積が前記第１の記憶制御用スイッチを構成するトランジスタのゲートの長さと幅との積の１／２でありドレインが前記電流記憶用トランジスタのゲートに接続されソースがドレインに短絡されたダミートランジスタを有することが好ましい。

【００４２】本発明は、近接領域にあるトランジスタの電流能力ばらつきが小さい場合に用いることができる。前記ｎビットデジタル／電流変換回路にある電流を記憶するトランジスタは、上述の本発明に係わる第１の半導体装置と同様な手段で電流を記憶する。ここで、前記電流を記憶するトランジスタと、前記電流を出力するトランジスタとカレントミラー構成であり、電流能力比が１：２：４：・・・：２ｎ－１であるｎ個の出力用トランジスタのうち、最も電流能力が大きいトランジスタとの電流能力比を、１：１又は２：１のように、電流を記憶するトランジスタを等しく、又は大きくすると、基準電流値が大きくなり、基準電流が流れる配線負荷を充放電する期間が短縮されるため、電流記憶期間を短くできる。この時、前記電流を記憶するトランジスタは、基準電流が流れた状態のゲートーソース電圧を記憶するため、電流能力のばらつきによらず、高い精度で電流を記憶できる。よって、近接領域にあるトランジスタの電流能力ばらつきが小さい場合、前記出力用トランジスタのドレインと前記ｎビットデジタル／電流変換回路の出力との間にデジタル入力画像データに従ってオン／オフするｎ個のスイッチを手段として備えることで、電流比が０、１、２、・・・、２ｎ－１となる精度の高い電流を出力することが可能となる。また、この場合、１つの基準電流源でｎビットデジタル／電流変換回路を構成でき、必要な入力を少なくすることができる。

【００４３】ここで、前記ゲートがバイアスされたバイアストランジスタを有する際には、前記電流記憶用トランジスタや前記電流出力用トランジスタと前記バイアストランジスタは、カスコード接続されており、共に飽和領域で動作する場合、ドレイン電流のドレイン電圧依存性を抑えることができるため、発光素子の特性がばらついても、供給される電流のばらつきを抑えることができる。

【００４４】本発明に係る第３の発光表示装置駆動用半導体装置は、供給される電流によって輝度が決まる発光素子が各画素に設けられた発光表示装置を駆動する発光

表示装置駆動用半導体装置において、前記発光素子の電流ー輝度特性に対応したｋ種の基準電流を記憶し前記記憶されたｋ種の基準電流から（ｎ－ｋ）種の電流を生成しこれらの電流の組み合わせからｎビットのデジタル画像データに基づいて２ｎ種の電流を出力するｎビットデジタル／電流変換回路を前記発光表示装置に電流を出力する出力端子毎に有することを特徴とする。

【００４５】なお、前記ｎビットデジタル／電流変換回路は、前記基準電流が流れるｋ本の信号線と、夫々に前記デジタル画像データの１ビットが伝達されるｎ本のデータ線と、制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続されたｋ個の電流記憶出力用トランジスタと、ゲートが前記ｋ個の電流記憶出力用トランジスタのうちのいずれか１つのゲートに短絡された（ｎ－ｋ）個の電流出力用トランジスタと、前記電流記憶出力用トランジスタのゲートと前記第２の電圧供給線との間に接続された１又は複数の容量素子と、夫々前記電流記憶出力用トランジスタ及び前記電流出力用トランジスタのドレインと出力端子との間に接続され前記データ線を伝達する信号のいずれかにより制御されるｎ個の出力制御用スイッチと、前記電流記憶出力用トランジスタのドレインと前記信号線との間に接続され前記制御線を伝達する信号により制御されるｋ個の第１の記憶制御用スイッチと、前記電流記憶出力用トランジスタのゲートとドレインとの間に接続され前記制御線を伝達する信号により制御されるｋ個の第２の記憶制御用スイッチと、を有し、前記各電流出力用トランジスタの電流能力は、全ての前記電流記憶出力用トランジスタのそれよりも低く、前記電流出力用トランジスタ及び前記電流記憶出力用トランジスタの電流能力は、夫々最も低い電流能力に対して順次２倍したものに設定されていてもよく、前記ｎビットデジタル／電流変換回路は、前記基準電流が流れるｋ本の信号線と、夫々に前記デジタル画像データの１ビットが伝達されるｎ本のデータ線と、第１及び第２の制御線と、第１及び第２の電圧供給線と、ソースが前記第１の電圧供給線に接続されたｋ個の電流記憶出力用トランジスタと、ゲートが前記ｋ個の電流記憶出力用トランジスタのうちのいずれか１つのゲートに短絡された（ｎ－ｋ）個の電流出力用トランジスタと、前記電流記憶出力用トランジスタのゲートと前記第２の電圧供給線との間に接続された１又は複数の容量素子と、夫々前記電流記憶出力用トランジスタ及び前記電流出力用トランジスタのドレインと出力端子との間に接続され前記データ線を伝達する信号のいずれかにより制御されるｎ個の出力制御用スイッチと、前記電流記憶出力用トランジスタのドレインと前記信号線との間に接続され前記第２の制御線を伝達する信号により制御されるｋ個の第１の記憶制御用スイッチと、前記電流記憶出力用トランジスタのゲートとドレインとの間に接続され前記第１の制御線を伝達する信号により制御されるｋ個の第２の記憶制御用スイッチと、を有し、前記各電流出力用トランジスタの電流能力は、全ての前記電流記憶出力用トランジスタのそれよりも低く、前記電流出力用トランジスタ及び前記電流記憶出力用トランジスタの電流能力は、夫々最も低い電流能力に対して順次２倍したものに設定されていてもよい。

【００４６】あるいは、前記電流記憶用トランジスタや前記電流出力用トランジスタと前記第１の電圧供給線との間に、それぞれ、ゲートがバイアスされたバイアストランジスタを有しても良い。

【００４７】また、前記出力制御用スイッチがオフ状態で前記第１及び第２の記憶制御用スイッチがオン状態のときに、前記電流記憶出力用トランジスタは、そのゲートードレイン間が短絡されて飽和領域で動作し、その動作が安定した段階における前記電流記憶出力用トランジスタのゲートーソース間電圧は、前記基準電流をドレインーソース間に流すために必要な電圧となり、その値は前記電流かつ記憶出力用トランジスタの電流能力に従い決定され、その後前記第１及び第２の記憶制御用スイッチがオフ状態になると、前記容量素子に前記電流記憶出力用トランジスタのゲートーソース間電圧が保持され、この保持されたゲートーソース間電圧に基づく基準電流から前記電流出力用トランジスタ及び電流記憶かつ出力用トランジスタが夫々の電流能力に基づいた総計でｎ種の電流を流すことができる状態となり、前記電流出力用トランジスタ及び電流記憶出力用トランジスタが流すことができる電流を出力するか否かが前記ｎビットのデジタル画像データによって決定されてもよい。

【００４８】更に、前記第２の記憶制御用スイッチは、前記第１の記憶制御用スイッチがオフ状態になった後にオフ状態になることが好ましい。

【００４９】前記出力制御用スイッチ並びに第１及び第２の記憶制御用スイッチがトランジスタから構成されていてもよい。

【００５０】また、前記ｎビットデジタル／電流変換回路は、前記第２の制御線を伝達する信号の反転信号がゲートに入力されゲートの長さと幅との積が前記第１の記憶制御用スイッチを構成するトランジスタのゲートの長さと幅との積の１／２でありドレインが前記電流記憶かつ出力用トランジスタのゲートに接続されソースがドレインに短絡されたダミートランジスタを有することが好ましい。

【００５１】本発明は、近接領域にあるトランジスタの電流能力ばらつきがやや小さい場合に用いることができる。電流記憶期間において、ｎビットデジタル／電流変換回路手段にある１乃至数個の前記電流記憶かつ出力用トランジスタは、トランジスタと同数の基準電流を、上述と同様な手段で記憶する。従って、前記電流を記憶する１～数個のトランジスタは、高い精度の電流を出力できる。一方、前記電流を記憶かつ出力するトランジスタ

とカレントミラー構成である１～数個の出力用トランジスタは、前記基準電流よりも低い電流を出力するようにすることで、電流能力がばらついた場合でも、全体の中での影響を小さくできる。以上のような構成により、電流比が１：２：４：・・・：２ｎ－１である電流を高い精度で供給でき、前記電流を記憶かつ出力するトランジスタや前記出力用トランジスタのドレインと前記デジタル／電流変換回路の出力との間にデジタル入力画像データに従ってオン／オフするｎ個のスイッチを手段として備えることで、電流比が０、１、２、・・・、２ｎ－１となる精度の高い電流を出力することが可能となる。また、この場合、１乃至数個の基準電流源でデジタル／電流変換回路を構成でき、外部からの入力を少なくすることができる。

【００５２】ここで、前記ゲートがバイアスされたバイアストランジスタを有する際には、前記電流記憶用トランジスタや前記電流出力用トランジスタと前記バイアストランジスタは、カスコード接続されており、共に飽和領域で動作する場合、ドレイン電流のドレイン電圧依存性を抑えることができるため、発光素子の特性がばらついても、供給される電流のばらつきを抑えることができる。

【００５３】本発明は、上述の第１から３のいずれかのデジタル／電流変換回路手段を組み合わせて、ｎビットデジタル／電流変換回路手段を構成することができる。例えば、最も電流値の高いビットには第１の発明の前記１ビットデジタル／電流変換回路を用い、それ以下のビットには第２の発明の（ｎ－１）ビットデジタル／電流変換回路を用いることで、ばらつきの影響の大きい最も電流値が高いビットの精度が高い一方、基準電流が２種類であるｎビットデジタル／電流変換回路を構成できる。

【００５４】更に、本発明において、前記第１及び第２の電圧供給線が共通の電源線とされていてもよい。

【００５５】更にまた、前記出力端子の数がａ、前記発光表示装置の画素の発光色がｂ色である場合、基準電流値はｎ×ｂ種必要となるが、この時、電流記憶動作がａ／ｂ回に分けて行われてもよく、１出力に相当するデジタル／電流変換回路が２個の前記ｎビットデジタル／電流変換回路を有することで、任意のフレームにおいて、一方を電流出力用回路とし、他方を電流記憶用回路とし、電流の記憶は各フレーム内で同じ基準電流を用いてａ／ｂ回に分けて行われ、フレーム毎に電流出力と電流記憶との役割が入れ替えられることがより好ましい。１フレームごとに枠割りを入れ替えることにより、発光表示装置を駆動する期間の他に電流を記憶するための期間を必要としない。よって、駆動する期間は、フレーム期間全体と考えることができ、１ラインを駆動する１水平期間を長く取ることができ、画素回路に高精度な電流を駆動することが可能となる。上述の動作は、例えば、前記１出力に相当するデジタル／電流変換回路が前記ｎビットデジタル／電流変換回路を３個以上備えた場合でも、同様である。また、電流出力と電流記憶の役割の入れ替えを行うのは、複数フレーム毎でも良い。

【００５６】本発明は、前記ｎビットデジタル／電流変換回路のような電流出力回路から出力される電流が入力されることで適当な電圧を出力するプリチャージ回路を有し、前記プリチャージ回路は、前記発光表示装置が単純マトリックス形式ならば前記発光素子と同等な負荷となり、前記発光表示装置がアクティブマトリックス方式ならば画素回路と同等な負荷となる擬似負荷回路と、前記擬似負荷回路に前記電流出力回路からの出力電流が流れた場合の電圧を入力とするボルテージフォロワと、前記電流出力回路の出力と前記擬似負荷回路との間に接続された第１のプリチャージ用スイッチと、前記第１のプリチャージ用スイッチを制御する信号を伝達する第１のプリチャージ用制御線と、前記電流出力回路の出力と前記発光表示装置とを接続する第２のプリチャージ用スイッチと、前記第２のプリチャージ用スイッチを制御し前記第１のプリチャージ用スイッチを制御する信号の反転信号を伝達する第２のプリチャージ用制御線と、前記ボルテージフォロワの出力と前記発光表示装置の間に接続され前記第１のプリチャージ用制御線を伝達する信号により制御される第３のスイッチと、を有することが好ましい。

【００５７】更に、１水平期間の初期にプリチャージ動作として前記擬似負荷回路に前記電流出力回路の出力電流を供給し、その電圧をボルテージフォロワを介して前記発光表示装置内の前記画素内の発光素子又は前記画素回路に印加し、その後電流駆動動作として前記電流出力回路の出力電流を直接前記発光表示装置内の前記画素内の発光素子又は前記画素回路に供給することにより、前記電流出力回路の出力電流が小さな場合でも、前記発光表示装置内の配線負荷等を充放電のための時間が短縮することができるため、前記発光表示装置内の前記画素内の発光素子又は前記画素回路をより安定かつ高速、高精度に駆動することができる。

【００５８】更にまた、前記プリチャージ回路に、前記ボルテージフォロワのオフセット電圧をキャンセルする構成を設けることにより、前記ボルテージフォロワのオフセット電圧をキャンセルする動作を、前記電流駆動動作時に行うことで、余分な時間が必要ない上に、前記電流を記憶・出力する回路の出力電流を前記擬似負荷回路に供給した場合と実際の前記発光表示装置内の画素（回路）に供給した場合の差が小さくなるため、前記発光表示装置内の前記画素内の発光素子又は前記画素回路を、より安定かつ高速、高精度に駆動することができる。

【００５９】プリチャージ回路を設けることにより、前記擬似の画素（回路）は、前記デジタル／電流変換回路の近くにあるため、その間の配線負荷は小さく、出力さ

れる電流が小さい場合でも、前記擬似の画素（回路）は、出力された電流を短い時間で安定に流すようになる。前記擬似の画素（回路）に電流が安定に流れている状態でのゲート電圧をボルテージフォロワに入力し、前記ボルテージフォロワの出力を発光表示装置のデータ線に接続することで、前記電流出力回路の出力電流が、前記表示部内の画素（回路）に安定に流れている状態の電圧に近い電圧が、前記信号線や前記表示部内の画素（回路）に印加される。以上のようなプリチャージ動作は、定電流で前記データ線の負荷を充放電するのに比べ、高速に行うことが可能である。プリチャージ動作により前記データ線と前記表示部内の画素（回路）の電圧が安定した後、前記電流出力回路と前記擬似の画素（回路）を切り離し、前記電流出力回路から直接前記データ線に電流を出力する。この場合、前記電流出力回路の出力である定電流による前記データ線の負荷や前記表示部内の画素（回路）の充放電は、既にプリチャージが行われているため、わずかに行うだけでよく、また、プリチャージ前の前記信号線の負荷や前記表示部内の画素（回路）の電圧などから影響を受けない。更に、駆動時間を短くすることができる。従って、以上のような２段階の駆動動作を行うことで、駆動前の発光表示部内の配線負荷や画素（回路）の負荷の電圧の影響を受けずに、安定、高速かつ高精度に画素（回路）を電流駆動することが可能となる。

【００６０】本発明に係る発光表示装置駆動用半導体装置は、出力ごとに、基準電流を記憶し、ｎビットデジタルデータに従って２ｎ種の電流を出力する前記ｎビットデジタル／電流変換回路を１つ又は複数備え、かつ、前記ｎビットデジタル／電流変換回路が電流の出力又は記憶動作を行うかにより、ｎビットデータラッチと、前記ｎビットデータラッチからのデータを前記ｎビットデジタル／電流変換回路に伝えるか否かを行うデータセレクタを備え、更に、装置全体として、前記基準電流を記憶する動作と同期した走査信号を出力する電流記憶用シフトレジスタを備える。更にまた、前記発光表示装置駆動用半導体装置は、出力ごとに前記プリチャージ回路を有する。更に、前記発光表示装置駆動用半導体装置は、外部から入力される入力されるｎビットデジタルデータをデータ保持用シフトレジスタの走査信号に同期して保持するｎビットデータレジスタを出力ごとに備え、装置全体として、前記データ保持用シフトレジスタを備える。また、１水平期間において前記ｎビットデジタル／電流回路又は前記プリチャージ回路の出力を、発光表示装置の複数のデータ線にセレクタ信号に従って順々に接続できる出力セレクタ回路をさらに備えることで、前記発光表示装置駆動用半導体装置は、より少ない回路規模で、発光表示装置を駆動することができる。

【００６１】なお、前記基準電流を生成する回路と共に１つのチップに集積されていてもよい。さらに、トランジスタが薄膜トランジスタで構成されても良い。

【００６２】本発明に係る発光表示装置は、前記発光素子と同じ基板に形成され前記基準電流を生成する回路と共に１つのチップに集積された上述のいずれかの発光表示装置駆動用半導体装置を有することを特徴とする。

【００６３】特に、前記発光素子と発光表示装置駆動用半導体装置が同じ基板に形成された場合には、前記プリチャージ回路内の擬似負荷（回路）は、表示装置の画素内の負荷（回路）と同一のサイズ、形状で構成できるため、得られるプリチャージ電圧の精度を高くすることができる。この時、上述のプリチャージ動作と電流出力動作を組み合わせた駆動法は、より安定、高速かつ高精度に駆動することができる。

【００６４】本発明の発光表示装置駆動用半導体装置及び発光表示装置は、前述の通り、発光素子の代わりに電流負荷素子で構成される、より一般的な、電流負荷素子や電流負荷デバイスを駆動するための半導体装置や電流負荷デバイスにも適用できる。

【００６５】

【発明の実施の形態】本発明の実施例に係る電流負荷デバイス用半導体装置について、上述と同様に発光表示装置用半導体装置を例にとり、添付の図面を参照して具体的に説明する。なお、以下の説明において、同じ構成要素で順序が設定されている場合は、アンダーバー及び数字を付して示し、個々に注目する場合には、アンダーバー及び数字を付さずに示している。

【００６６】図１は本発明の第１の実施例に係る発光表示装置用半導体装置の構成を示すブロック図である。第１の実施例には、デジタル／電流（Ｄ／Ｉ）変換部２１０が設けられており、このＤ／Ｉ変換部２１０に、発光表示装置への出力数（３×ｎ）分の１出力Ｄ／Ｉ変換部２３０、及び３出力毎に設けられたｎ個のフリップフロップ（Ｆ／Ｆ）２９０＿１乃至２９０＿ｎから構成されたシフトレジスタが設けられている。シフトレジスタには、電流を記憶するタイミング制御のためのスタート信号ＩＳＴ、クロック信号ＩＣＬ、及びこのクロック信号ＩＣＬの反転信号ＩＣＬＢが入力される。また、１出力Ｄ／Ｉ変換部２３０には、各出力のデジタル画像データＤ０乃至Ｄ２が入力され、参照するための基準電流ＩＲ０乃至ＩＲ２、ＩＧ０乃至ＩＧ２、ＩＢ０乃至ＩＢ２のいずれかがそれに割り当てられた発光色に応じて入力される。また、基準電流は、発光色が赤、青、緑である夫々の発光素子の電流－輝度特性にあった電流値であり、基準電流ＩＲ０の電流値ｉｒ０は発光色が赤の発光素子の１階調目に対応し、基準電流ＩＲ１の電流値ｉｒ１は発光色が赤の発光素子の２階調目に対応し、基準電流ＩＲ２の電流値ｉｒ２は発光色が赤の４階調目に対応する。同様に、基準電流ＩＧ０乃至ＩＧ２の電流値は、夫々発光色が緑の１階調目、２階調目、４階調目に対応し、基準電流ＩＢ０乃至ＩＢ２は、夫々発光色が青の１

階調目、２階調目、４階調目に対応する。１個のＦ／Ｆ２９０と、このＦ／Ｆ２９０から出力された信号ＭＳＷが入力される３個の１出力Ｄ／Ｉ変換部２３０とから１個のＲＧＢ　Ｄ／Ｉ変換部２２０が構成されている。

【００６７】図２は１出力Ｄ／Ｉ変換部２３０の構成を示すブロック図である。１出力Ｄ／Ｉ変換部２３０は３個の１ビットＤ／Ｉ変換部２３１から構成されている。これらの１ビットＤ／Ｉ変換部２３１には、夫々画像データＤ０及び基準電流Ｉ０の組み合わせ、画像データＤ１及び基準電流Ｉ１の組み合わせ、画像データＤ２及び基準電流Ｉ２の組み合わせのいずれかが入力されると共に、Ｆ／Ｆの出力信号である信号ＭＳＷが入力される。なお、基準電流Ｉ０乃至Ｉ２は、基準電流ＩＲ０乃至ＩＲ２の組み合わせ、基準電流ＩＧ０乃至ＩＧ２の組み合わせ、基準電流ＩＢ０乃至ＩＢ２の組み合わせのいずれかに対応する。つまり、赤（Ｒ）表示用の１出力Ｄ／Ｉ変換部２３０において、デジタル階調データＤ０が入力される１ビットＤ／Ｉ変換部２３１に供給される基準電流は、赤表示用の発光素子の１階調目の輝度に対応する基準電流ＩＲ０である。また、デジタル階調データＤ１が入力される１ビットＤ／Ｉ変換部２３１に供給される基準電流は、赤表示用の発光素子の２階調目の輝度に対応する基準電流ＩＲ１であり、デジタル階調データＤ２が入力される１ビットＤ／Ｉ変換部２３１に供給される基準電流は、赤表示用の発光素子の４階調目の輝度に対応する基準電流ＩＲ２である。但し、発光素子の電流ー輝度特性が比例関係を有するので、ｉｒ１＝２×ｉｒ０及びｉｒ２＝４×ｉｒ０の関係が成り立つ。同様に、緑（Ｇ）表示用又は青（Ｂ）表示用の１出力Ｄ／Ｉ変換部２３０に設けられている１ビットＤ／Ｉ変換部２３１であって、階調データＤ０、Ｄ１、Ｄ２が入力されるものには、夫々基準電流ＩＧ０又はＩＢ０、基準電流ＩＧ１又はＩＢ１、基準電流ＩＧ２又はＩＢ２が入力される。

【００６８】図３は１ビットＤ／Ｉ変換部２３１の構成を示すブロック図である。１ビットＤ／Ｉ変換部２３１には、電流記憶・出力用のトランジスタＮチャネル薄膜トランジスタ（ＴＦＴ）Ｔ１、スイッチＳＷ１乃至ＳＷ３及び容量素子Ｃ１が設けられている。スイッチＳＷ１はＴＦＴＴ１のドレインに接続されており、階調データＤ＊により制御される。スイッチＳＷ１の他端から、出力電流Ｉｏｕｔが出力される。スイッチＳＷ２は、スイッチＳＷ１とＴＦＴＴ１との接点と、容量素子Ｃ１の一端及びＴＦＴＴ１のゲートとの間に接続されており、信号ＭＳＷにより制御される。スイッチＳＷ３の一端は基準電流Ｉ＊が供給される信号線に接続され、その他端はスイッチＳＷ１とＴＦＴＴ１との接点と容量素子Ｃ１の一端との間に接続されており、信号ＭＳＷにより制御される。また、ＴＦＴＴ１のソース及び容量素子Ｃ１の他端は、例えば接地されているが、動作上問題がない場合には、接地電圧ＧＮＤよりも高い電圧が供給されてもよい。なお、階調データＤ＊及び基準電流Ｉ＊は、階調データＤ０及び基準電流Ｉ０、階調データＤ１及び基準電流Ｉ１、階調データＤ２及び基準電流Ｉ２のいずれかに相当する。

【００６９】次に、上述のように構成された第１の実施例に係る発光表示装置用半導体装置の動作について説明する。図４は本発明の第１の実施例に係る発光表示装置用半導体装置の動作を示すタイミングチャートである。図４中のＹ＿１及びＹ＿２は、夫々垂直走査回路３００（図３５参照）の第１行目、第２行目の出力信号を示し、Ｄ０、Ｄ１、Ｄ２は３ビットデジタル画像データ（階調データ）を示し、Ｉｏｕｔは１出力Ｄ／Ｉ変換部２３０の出力信号を示し、ＩＳＴはｎ個のフリップフロップ２９０から構成されるシフトレジスタのスタート信号を示し、ＩＣＬはシフトレジスタのクロック信号を示し、ＭＳＷ＿１、ＭＳＷ＿２は、夫々シフトレジスタの第１段目、第２段目の出力信号を示す。

【００７０】表示部４００（図３５参照）を垂直走査し始めてから、次の垂直走査が始まるまでを１フレームとする。１フレームは、電流駆動期間（第１の動作期間）及び電流記憶期間（第２の動作期間）から構成される。

【００７１】先ず、電流記憶期間（第２の動作期間）について説明する。電流記憶期間において、各１ビットＤ／Ｉ変換部２３１は夫々に基準電流源から供給された基準電流を記憶する。ここで、本期間においては、全デジタル階調データをロウレベルとし、１ビットＤ／Ｉ変換部２３１のスイッチＳＷ１は、オフである。

【００７２】電流記憶期間の開始と共に、スタート信号ＩＳＴとしてパルス信号が第１段目のＦ／Ｆ２９０＿１に入力され、このパルス信号の入力と同時に、クロック信号ＩＣＬ及びクロック反転信号ＩＣＬＢがＦ／Ｆ２９０＿１に入力されることで、ｎ個のＦ／Ｆ２９０から構成されるシフトレジスタが動作し始める。第１段目のＦ／Ｆ２９０＿１の出力信号ＭＳＷ＿１がハイレベルになると、この出力信号ＭＳＷ＿１が入力される１出力Ｄ／Ｉ変換部２３０に設けられた各１ビットＤ／Ｉ変換部２３１のスイッチＳＷ２及びＳＷ３がオンとなる。スイッチＳＷ２及びＳＷ３がオンになると、その１ビットＤ／Ｉ変換部２３１内の電流記憶・出力用ＴＦＴＴ１は、そのゲートードレイン間がショートされるため、飽和領域で動作する。そして、本動作が安定した状態では、ＴＦＴＴ１のドレインーソース間に基準電流源からの基準電流が流れるように、ＴＦＴＴ１の電流能力に合わせてそのゲート電圧が設定される。

【００７３】安定状態になった後に、信号ＭＳＷ＿１がロウレベルになると共に、第２段目のＦ／Ｆの出力信号ＭＳＷ＿２がハイレベルになると、Ｆ／Ｆ２９０＿１が設けられたＲＧＢ　Ｄ／Ｉ変換部２２０内の各１ビットＤ／Ｉ変換部２３１のスイッチＳＷ２及びＳＷ３がオフになる。この時、Ｆ／Ｆ２９０＿１が設けられたＲＧＢ

Ｄ／Ｉ変換部２２０内のＴＦＴＴ１のゲート電圧は、容量素子Ｃ１によって基準電流が流れるような電圧に保持される。この結果、ＴＦＴＴ１には、夫々の電流能力に関わらず、基準電流が記憶される。このような、信号ＭＳＷがハイレベルとなっている期間を、そのＲＧＢ Ｄ／Ｉ変換部２２０における３出力電流記憶期間とする。一方、第２段目のＦ／Ｆが設けられたＲＧＢ Ｄ／Ｉ変換部２２０内の各スイッチＳＷ２及びＳＷ３はオンとなり、安定した状態では、ＴＦＴＴ１のドレインーソース間に基準電流が流れるように飽和領域で動作し、その基準電流が流れるように、ＴＦＴＴ１の電流能力に合わせてゲート電圧が設定される。

【００７４】電流記憶期間では、上述のような３出力電流記憶期間が、全てのＲＧＢ Ｄ／Ｉ変換部２２０について繰り返され、全ての１出力Ｄ／Ｉ変換部２３０に基準電流が記憶される。

【００７５】次に、電流駆動期間（第１の動作期間）について説明する。電流駆動期間において、垂直走査回路３００が１行ずつ制御線（走査線）を選択していく。図４には、第１行目、第２行目の出力である走査パルスＹ＿１及びＹ＿２を示している。

【００７６】走査パルスＹ＿１がハイレベルになると、第１行目の制御線が選択され、これに同期して出力数分の第１行目の３ビットデジタル階調データＤ０乃至Ｄ２が出力毎に１出力Ｄ／Ｉ変換部２３０に入力される。デジタル階調データＤ０乃至Ｄ２が入力されると、これらのレベル（ハイレベル（Ｈ）／ロウレベル（Ｌ））に応じて１ビットＤ／Ｉ変換部２３１内のスイッチＳＷ１のオン／オフが制御され、直前のフレームの電流駆動期間でＴＦＴＴ１に記憶されていた電流が出力される。下記表１に入力デジタル階調データＤ０乃至Ｄ２と階調（出力電流値）との関係を示す。

【００７７】

【表１】

階調	階調データ			出力電流値（Ｉｏｕｔの電流値）
	Ｄ０	Ｄ１	Ｄ２	
０	Ｌ	Ｌ	Ｌ	０
１	Ｈ	Ｌ	Ｌ	ｉ０
２	Ｌ	Ｈ	Ｌ	ｉ１＝２×ｉ０
３	Ｈ	Ｈ	Ｌ	ｉ１＋ｉ０＝３×ｉ０
４	Ｌ	Ｌ	Ｈ	ｉ２＝４×ｉ０
５	Ｈ	Ｌ	Ｈ	ｉ２＋ｉ０＝５×ｉ０
６	Ｌ	Ｈ	Ｈ	ｉ２＋ｉ１＝６×ｉ０
７	Ｈ	Ｈ	Ｈ	ｉ２＋ｉ１＋ｉ０＝７×ｉ０

【００７８】表１に示すように、出力電流値は、０から７×ｉ０まで、入力されるデジタル階調データによって、調整することができる。また、電流記憶期間（第２の動作期間）でＴＦＴＴ１の電流能力に合わせて、基準電流源と同等な電流が流れるようにゲート電圧が設定され、同じＴＦＴＴ１を使用して電流が出力されているため、電流能力のばらつきに関係なく、出力電流のばらつきは小さく、高い精度が得られる。

【００７９】一方、電流駆動期間（第１の動作期間）では、シフトレジスタは動作せず、全てのスイッチＳＷ２及びＳＷ３は常にオフのままである。

【００８０】そして、以上のような動作を各フレームについて繰り返すことにより、表示部４００において階調データＤ０乃至Ｄ２に応じた表示が行われ、その際、高精度な電流が画素回路に供給される。

【００８１】このような第１の実施例によれば、図３８（ａ）に示すようなＰチャネルＴＦＴを有する発光表示装置に対し、高速かつ高い精度で電流を供給することができる。

【００８２】次に、本発明の第２の実施例について説明

する。第２の実施例は、第１の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ｂ）に示す画素回路に対して適用されるものである。図５は本発明の第２の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【００８３】第２の実施例における１ビットＤ／Ｉ変換部２３１ａには、第１の実施例におけるＮチャネルＴＦＴＴ１に代わってＰチャネルＴＦＴＴ２が設けられており、そのソース及び容量素子Ｃ１の一端に電源電位ＶＤが供給される。電圧ＶＤは、電圧ＶＥＬと同程度か、又は低い電圧で、動作に問題がないレベルとする。

【００８４】第１の実施例は、図３８（ａ）に示すような画素回路の電流を流すトランジスタがＰチャネルＴＦＴである場合に適用可能なものであるが、第２の実施例は、図３８（ｂ）に示すようなＮチャネルＴＦＴに適用可能である。つまり、画素回路内のＴＦＴがＰチャネルＴＦＴである場合には、そのソース電圧は電圧ＶＥＬであるが、ＮチャネルＴＦＴとした場合には、そのソース電圧を接地レベルＧＮＤにする必要があり、本実施例はこれに対応することができる。

【００８５】なお、第２の実施例の動作は、出力電流の極性が変わることを除き、第１の実施例と同様であり、同様の効果が得られる。

【００８６】次に、本発明の第３の実施例について説明する。第３の実施例は、第１の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ａ）に示す画素回路に対して適用されるものである。図６は本発明の第３の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【００８７】第３の実施例における１ビットＤ／Ｉ変換部２３１ｂにおいては、容量素子Ｃ１の一端に接地電位ＧＮＤではなく、適当な安定電圧ＶＢが供給される。

【００８８】第３の実施例の動作は、第１の実施例と同様であり、同様の効果が得られる。このことは、容量素子Ｃ１に供給される電圧は、安定したものであれば、どのような電圧でも良いことを示している。

【００８９】次に、本発明の第４の実施例について説明する。第４の実施例は、第１の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ｂ）に示す画素回路に対して適用されるものである。図７は本発明の第４の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【００９０】第４の実施例における１ビットＤ／Ｉ変換部２３１ｃにおいては、第３の実施例と同様に、容量素子Ｃ１の一端に接地電位ＧＮＤではなく、適当な安定電圧ＶＢが供給される。また、第２の実施例と同様に、第１の実施例におけるＮチャネルＴＦＴＴ１に代わってＰチャネルＴＦＴＴ２が設けられており、そのソース及び容量素子Ｃ１の一端に電源電位ＶＤが供給される。

【００９１】このように、第４の実施例は第２の実施例に第３の実施例を適用したようなものであり、第３の実施例と同様に、容量素子Ｃ１に供給される電圧は、安定したものであれば、どのような電圧でも良いことを示している。

【００９２】次に、本発明の第５の実施例について説明する。第５の実施例は、第１の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ａ）に示す画素回路に対して適用されるものである。図８は本発明の第５の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【００９３】第５の実施例における１ビットＤ／Ｉ変換部２３１ｄには、第１の実施例におけるスイッチＳＷ１乃至ＳＷ３に代わって、夫々Ｎチャネルトランジスタ１１乃至１３が設けられている。

【００９４】このような第５の実施例によっても、図４に示すタイミングチャートに基づいて第１の実施例と同様の動作が行われ、同様の効果が得られる。なお、ＮチャネルトランジスタＴ１１乃至Ｔ１３の代わりにＰチャネルトランジスタを使用することもできる。この場合には、タイミングチャートは、Ｆ／Ｆの出力信号を図４に示すものを反転したものとすればよい。

【００９５】次に、本発明の第６の実施例について説明する。第６の実施例は、第１の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ｂ）に示す画素回路に対して適用されるものである。図９は本発明の第６の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【００９６】第６の実施例における１ビットＤ／Ｉ変換部２３１ｅには、第２の実施例におけるスイッチＳＷ１乃至ＳＷ３に代わって、夫々Ｎチャネルトランジスタ１１乃至１３が設けられている。

【００９７】このような第６の実施例によっても、図４に示すタイミングチャートに基づいて第２の実施例と同様の動作が行われ、同様の効果が得られる。なお、ＮチャネルトランジスタＴ１１乃至Ｔ１３の代わりにＰチャネルトランジスタを使用することもできる。この場合には、タイミングチャートは、Ｆ／Ｆの出力信号を図４に示すものを反転したものとすればよい。

【００９８】次に、本発明の第７の実施例について説明する。第７の実施例は、例えば図３８（ａ）に示す画素回路に対して適用されるものである。図１０は本発明の第７の実施例に係る発光表示装置用半導体装置の構成を示すブロック図である。

【００９９】第７の実施例には、Ｄ／Ｉ変換部２１０ａが設けられており、このＤ／Ｉ変換部２１０ａに、発光表示装置への出力数（３×ｎ）分の１出力Ｄ／Ｉ変換部２３０ａ、及び３出力毎に設けられたｎ個のフリップフロップ（Ｆ／Ｆ）２９０ａ＿１乃至２９０ａ＿ｎから構成されたシフトレジスタが設けられている。シフトレジスタには、電流を記憶するタイミング制御のためのスタ

ート信号ＩＳＴ、クロック信号ＩＣＬ、このクロック信号ＩＣＬの反転信号ＩＣＬＢ、及び電流記憶タイミング信号ＩＴが入力される。また、１出力Ｄ／Ｉ変換部２３０ａには、各出力のデジタル画像データＤ０乃至Ｄ２が入力され、参照するための基準電流ＩＲ０乃至ＩＲ２、ＩＧ０乃至ＩＧ２、ＩＢ０乃至ＩＢ２のいずれかがそれに割り当てられた発光色に応じて入力される。１個のＦ／Ｆ２９０ａと、このＦ／Ｆ２９０ａから出力された信号ＭＳＷ１及びＭＳＷ２が入力される３個の１出力Ｄ／Ｉ変換部２３０ａとから１個のＲＧＢ　Ｄ／Ｉ変換部２２０ａが構成されている。

【０１００】図１１は１出力Ｄ／Ｉ変換部２３０ａの構成を示すブロック図である。１出力Ｄ／Ｉ変換部２３０ａは３個の１ビットＤ／Ｉ変換部２３１ｆから構成されている。これらの１ビットＤ／Ｉ変換部２３１ｆには、夫々画像データＤ０及び基準電流Ｉ０の組み合わせ、画像データＤ１及び基準電流Ｉ１の組み合わせ、画像データＤ２及び基準電流Ｉ２の組み合わせのいずれかが入力されると共に、Ｆ／Ｆの出力信号である信号ＭＳＷ１及びＭＳＷ２が入力される。

【０１０１】図１２は１ビットＤ／Ｉ変換部２３１ｆの構成を示すブロック図である。１ビットＤ／Ｉ変換部２３１ｆには、第５の実施例と同様に、電流記憶・出力用のトランジスタＮチャネルＴＦＴＴ１、Ｎチャネルトランジスタ１１乃至１３及び容量素子Ｃ１が設けられている。トランジスタＴ１１、Ｔ１２、Ｔ１３のゲートには、夫々階調データＤ０、信号ＭＳＷ２、信号ＭＳＷ１が入力され、各トランジスタはこれらの信号により制御される。

【０１０２】次に、上述のように構成された第７の実施例に係る発光表示装置用半導体装置の動作について説明する。図１３は本発明の第７の実施例に係る発光表示装置用半導体装置の動作を示すタイミングチャートである。

【０１０３】本実施例においては、図１３に示すように、電流記憶期間において、信号ＭＳＷ１は、第１の実施例における信号ＭＳＷと同様に変化する。また、電流記憶タイミング信号ＩＴは、いずれかの信号ＭＳＷ１の立ち上がりに同期して立ち上がり、その信号ＭＳＷ１よりも早いタイミングで立ち下がる。そして、信号ＭＳＷ２は、信号ＭＳＷ１と同じタイミングで立ち上がり、電流記憶タイミング信号ＩＴの立ち下がりに同期して立ち下がる。信号ＭＳＷ２が立ち上がっている期間を、そのＲＧＢ　Ｄ／Ｉ変換部２２０ａにおける３出力電流記憶期間とする。

【０１０４】このような第７の実施例では、１ビットＤ／Ｉ変換部２３１ｆは、３出力電流記憶期間終了時にトランジスタＴ１２のみがオフし、その後トランジスタＴ１３がオフする。従って、ドレインーソース間に基準電流を安定に流している状態のＴＦＴＴ１のゲート電圧は、トランジスタＴ１３がオフする際のノイズの影響を受けず、より正確に保持される。このため、本実施例は、第５の実施例と比してより一層精度の高い電流を供給することができる。

【０１０５】次に、本発明の第８の実施例について説明する。第８の実施例は、第７の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ｂ）に示す画素回路に対して適用されるものである。図１４は本発明の第８の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【０１０６】第８の実施例における１ビットＤ／Ｉ変換部２３１ｇには、第７の実施例におけるＮチャネルＴＦＴＴ１の代わってＰチャネルＴＦＴＴ２が設けられており、そのソース及び容量素子Ｃ１の一端に電源電位ＶＤが供給される。

【０１０７】なお、第８の実施例の動作は、出力電流の極性が変わることを除き、第７の実施例と同様であり、同様の効果が得られる。例えば第６の実施例と比してより一層精度の高い電流を供給することができる。

【０１０８】次に、本発明の第９の実施例について説明する。第９の実施例は、例えば図３８（ａ）に示す画素回路に対して適用されるものである。図１５は本発明の第９の実施例に係る発光表示装置用半導体装置の構成を示すブロック図である。

【０１０９】第９の実施例には、Ｄ／Ｉ変換部２１０ｂが設けられており、このＤ／Ｉ変換部２１０ｂに、発光表示装置への出力数（３×ｎ）分の１出力Ｄ／Ｉ変換部２３０ｂ、及び３出力毎に設けられたｎ個のフリップフロップ（Ｆ／Ｆ）２９０ｂ＿１乃至２９０ｂ＿ｎから構成されたシフトレジスタが設けられている。シフトレジスタには、電流を記憶するタイミング制御のためのスタート信号ＩＳＴ、クロック信号ＩＣＬ、このクロック信号ＩＣＬの反転信号ＩＣＬＢ、及び電流記憶タイミング信号ＩＴが入力される。また、１出力Ｄ／Ｉ変換部２３０ｂには、各出力のデジタル画像データＤ０乃至Ｄ２が入力され、参照するための基準電流ＩＲ０乃至ＩＲ２、ＩＧ０乃至ＩＧ２、ＩＢ０乃至ＩＢ２のいずれかがそれに割り当てられた発光色に応じて入力される。１個のＦ／Ｆ２９０ｂと、このＦ／Ｆ２９０ｂから出力された信号ＭＳＷ１、ＭＳＷ２及びＭＳＷ２Ｂが入力される３個の１出力Ｄ／Ｉ変換部２３０ｂとから１個のＲＧＢ　Ｄ／Ｉ変換部２２０ｂが構成されている。なお、信号ＭＳＷ２Ｂは信号ＭＳＷ２の反転信号である。

【０１１０】図１６は１出力Ｄ／Ｉ変換部２３０ｂの構成を示すブロック図である。１出力Ｄ／Ｉ変換部２３０ｂは３個の１ビットＤ／Ｉ変換部２３１ｈから構成されている。これらの１ビットＤ／Ｉ変換部２３１ｈには、夫々画像データＤ０及び基準電流Ｉ０の組み合わせ、画像データＤ１及び基準電流Ｉ１の組み合わせ、画像データＤ２及び基準電流Ｉ２の組み合わせのいずれかが入力

されると共に、Ｆ／Ｆの出力信号である信号ＭＳＷ１、ＭＳＷ２及びＭＳＷ２Ｂが入力される。

【０１１１】図１７は１ビットＤ／Ｉ変換部２３１ｈの構成を示すブロック図である。１ビットＤ／Ｉ変換部２３１ｈには、第７の実施例と同様に、電流記憶・出力用のトランジスタＮチャネルＴＦＴＴ１、Ｎチャネルトランジスタ１１乃至１３及び容量素子Ｃ１が設けられている。トランジスタＴ１１、Ｔ１２、Ｔ１３のゲートには、夫々階調データＤ０、信号ＭＳＷ２、信号ＭＳＷ１が入力され、各トランジスタはこれらの信号により制御される。また、本実施例においては、Ｎチャネルトランジスタ１２と容量素子Ｃ１の一端との間にＮチャネルトランジスタＴ１４が接続されている。Ｎチャネルトランジスタ１４のソース及びドレインは、互いに短絡されており、そのゲートには信号ＭＳＷ２Ｂが入力される。そして、ＴＦＴＴ１のゲートは、Ｎチャネルトランジスタ１４のドレインと容量素子Ｃ１の一端との接点に接続されている。また、トランジスタＴ１４のトランジスタ長Ｌとトランジスタ幅Ｗとの積は、トランジスタＴ１２のトランジスタ長Ｌとトランジスタ幅Ｗとの積の半分である。

【０１１２】このように構成された第９の実施例に係る発光表示装置用半導体装置は、第７の実施例と同様に、図１３に示すタイミングチャートに基づいて動作する。但し、信号ＭＳＷ２Ｂの波形は、信号ＭＳＷ２の波形を反転させたものである。

【０１１３】従って、１ビットＤ／Ｉ変換部２３１ｈは、３出力電流記憶期間終了時にトランジスタＴ１２がオフすると同時にトランジスタＴ１４がオンし、これに遅れてトランジスタＴ１３がオフする。このため、ドレインーソース間に基準電流を安定に流している状態のＴＦＴＴ１のゲート電圧は、トランジスタＴ１３がオフする際のノイズの影響を受けず、また、トランジスタＴ１２がオフする際に生じる電荷の移動もトランジスタＴ１４のオンにより吸収され、より一層正確に保持される。このように、本実施例は、第７の実施例と比してより一層精度の高い電流を供給することができる。

【０１１４】次に、本発明の第１０の実施例について説明する。第１０の実施例は、第９の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ｂ）に示す画素回路に対して適用されるものである。図１８は本発明の第１０の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【０１１５】第１０の実施例における１ビットＤ／Ｉ変換部２３１ｉには、第９の実施例におけるＮチャネルＴＦＴＴ１の代わってＰチャネルＴＦＴＴ２が設けられており、そのソース及び容量素子Ｃ１の一端に電源電位ＶＤが供給される。

【０１１６】なお、第１０の実施例の動作は、出力電流の極性が変わることを除き、第９の実施例と同様であり、同様の効果が得られる。例えば第８の実施例と比してより一層精度の高い電流を供給することができる。

【０１１７】次に、本発明の第１１の実施例について説明する。第１１の実施例は、第１の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ａ）に示す画素回路に対して適用されるものである。図３０は本発明の第１１の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【０１１８】第１１の実施例における１ビットＤ／Ｉ変換部２３１ｊにおいては、ＳＷ２の両端が、それぞれ、スイッチＳＷ１とＴＦＴ１の接点とＴＦＴＴ１のゲートに接続されるのではなく、基準電流Ｉ＊が供給される信号線とＴＦＴＴ１のゲートに接続されている。

【０１１９】第１１の実施例の動作は、第１の実施例と同様であり、同様の効果が得られる。また第１の実施例に対する第２乃至第１０の実施例のような変更を行うことができる。

【０１２０】次に、本発明の第１２の実施例について説明する。第１２の実施例は、第１の実施例における１ビットＤ／Ｉ変換部の構成を変更したものであり、例えば図３８（ａ）に示す画素回路に対して適用されるものである。図３１は本発明の第１２の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【０１２１】第１２の実施例における１ビットＤ／Ｉ変換部２３１ｋにおいては、ＴＦＴＴ１とＧＮＤ線の間にＴＦＴＴ１５が追加され、ＴＦＴ１５のゲートには適当な電圧ＶＳ１が印加されている。

【０１２２】第１２の実施例の動作は、第１の実施例と同様であり、同様の効果が得られる。また実施例は、追加されたＴＦＴＴ１５とＴＦＴＴ１がカスコード接続されているため、ＴＦＴ１の飽和領域におけるドレイン電流のドレイン電圧依存性が平坦化され、出力電流Ｉｏｕｔの精度を高めることが可能となる。されに本実施例は、第１の実施例に対する第２乃至第１０の実施例のような変更を行うことができる。

【０１２３】次に、本発明の第１３の実施例について説明する。第１１の実施例は、例えば図３８（ａ）に示す画素回路に対して適用されるものであり、近接領域の電流能力ばらつきが小さい場合に使用することができる。図１９は本発明の第１３の実施例に係る発光表示装置用半導体装置の構成を示すブロック図である。

【０１２４】第１３の実施例には、Ｄ／Ｉ変換部２１０ｃが設けられており、このＤ／Ｉ変換部２１０ｃに、発光表示装置への出力数（３×ｎ）分の１出力Ｄ／Ｉ変換部２３０ｃ、及び３出力毎に設けられたｎ個のフリップフロップ（Ｆ／Ｆ）２９０＿１乃至２９０＿ｎから構成されたシフトレジスタが設けられている。シフトレジスタには、電流を記憶するタイミング制御のためのスタート信号ＩＳＴ、クロック信号ＩＣＬ、及びこのクロック信号ＩＣＬの反転信号ＩＣＬＢが入力される。また、１

出力Ｄ／Ｉ変換部２３０ｃには、各出力のデジタル画像データＤ０乃至Ｄ２が入力され、参照するための基準電流ＩＲ２、ＩＧ２、ＩＢ２のいずれかがそれに割り当てられた発光色に応じて入力される。１個のＦ／Ｆ２９０と、このＦ／Ｆ２９０から出力された信号ＭＳＷが入力される３個の１出力Ｄ／Ｉ変換部２３０ｃとから１個のＲＧＢ　Ｄ／Ｉ変換部２２０ｃが構成されている。

【０１２５】なお、基準電流の電流値は、発光色が赤、青、緑である夫々の電流輝度特性に合わせており、基準電流ＩＲ２の電流値ｉｒ２は発光色が赤の４階調目に対応し、基準電流ＩＧ２の電流値ｉｇ２は発光色が緑の４階調目に対応し、基準電流ＩＢ２の電流値ｉｂ２は、発光色が青の４階調目に対応している。つまり、赤（Ｒ）表示用の１出力Ｄ／Ｉ変換部２３０ｃに供給される基準電流は赤表示用の発光素子の４階調目の輝度に対応する基準電流ＩＲ２である。但し、発光素子の電流－輝度特性が比例関係を有するので、１階調目に対応する電流値をｉｒ０とすると、ｉｒ２＝４×ｉｒ０となる。同様に、緑（Ｇ）表示用又は青（Ｂ）表示用の１出力Ｄ／Ｉ変換部２３０ｃには、夫々基準電流ＩＧ２又はＩＢ２が入力される。従って、本実施例では、入力される基準電流の最小値は、第１の実施例の４倍となる。なお、基準電流を４階調目に対応させた理由は、後述のように、１出力Ｄ／Ｉ変換部２３０ｃに設けられる電流を記憶するＮチャネルＴＦＴＴ２３の電流能力と、４階調目に相当する電流を出力するＮチャネルＴＦＴＴ２２の電流能力とを等しくなるように設計したためである。

【０１２６】図２０は１出力Ｄ／Ｉ変換部２３０ｃの構成を示すブロック図である。１出力Ｄ／Ｉ変換部２３０ｃには、信号ＭＳＷにより制御されその一端に基準電流Ｉ＊が供給されるスイッチＳＷ２３ａが設けられている。スイッチ２３ａの他端には、ＮチャネルＴＦＴＴ２３のドレイン及びゲートが共通接続されている。ＴＦＴＴ２３のソースは接地されている。ＮチャネルＴＦＴＴ２３のドレイン及びゲートに、信号ＭＳＷにより制御されるスイッチＳＷ２３ｂの一端が接続され、他端にＮチャネルＴＦＴＴ２０乃至Ｔ２２のゲート及び容量素子Ｃ２の一端が共通接続されている。ＴＦＴＴ２０乃至Ｔ２２のソース及び容量素子Ｃ２の他端は接地されている。ＴＦＴＴ２０、Ｔ２１、Ｔ２２のドレインには、夫々階調データＤ０、Ｄ１、Ｄ２により制御されるスイッチＳＷ２０、ＳＷ２１、ＳＷ２２が接続されており、これらのスイッチＳＷ２０乃至ＳＷ２２の他端が共通接続されている。この共通接続点から、出力電流Ｉｏｕｔが出力される。なお、ＴＦＴＴ２０、Ｔ２１、Ｔ２２の電流能力比は１：２：４となっている。また、ＴＦＴＴ２２の電流能力とＴＦＴＴ２３の電流能力とは、互いに同じになるように設計する。なお、動作上問題がない場合には、ＴＦＴＴ２０乃至Ｔ２３のソース及び容量素子Ｃ２の一端には接地電位ＧＮＤではなく、接地電位ＧＮＤよりも高い電圧が供給されても良い。例えば容量素子Ｃ２のみが異なる信号線に接続されていてもよい。

【０１２７】このように構成された第１３の実施例に係る発光表示装置用半導体装置は、第１の実施例と同様に、図４に示すタイミングチャートに基づいて動作する。

【０１２８】第１３の実施例における電流記憶期間（第２の動作期間）において、各１出力Ｄ／Ｉ変換部２３０ｃは夫々に基準電流源から供給された基準電流（ＩＲ２、ＩＧ２又はＩＢ２のいずれか）を記憶する。ここで、本期間においては、全デジタル階調データをロウレベルとし、１出力Ｄ／Ｉ変換部２３０ｃのスイッチＳＷ２０乃至ＳＷ２２は、オフである。

【０１２９】電流記憶期間の開始と共に、スタート信号ＩＳＴとしてパルス信号が第１段目のＦ／Ｆ２９０＿１に入力され、このパルス信号の入力と同時に、クロック信号ＩＣＬ及びクロック反転信号ＩＣＬＢがＦ／Ｆ２９０＿１に入力されることで、ｎ個のＦ／Ｆ２９０から構成されるシフトレジスタが動作し始める。第１段目のＦ／Ｆ２９０＿１の出力信号ＭＳＷ＿１がハイレベルになると、このＦ／Ｆ２９０＿１が設けられているＲＧＢ　Ｄ／Ｉ変換部２２０ｃ内の１出力Ｄ／Ｉ変換部２３０ｃに設けられているスイッチＳＷ２３ａ及びＳＷ２３ｂがオンとなる。スイッチＳＷ２３ａ及びＳＷ２３ｂがオンとなると、１出力Ｄ／Ｉ変換部２３０ｃの電流記憶用ＴＦＴＴ２３は、そのゲートードレイン間がショートされているため、飽和領域で動作する。その後、安定状態になると、ＴＦＴＴ２３のドレインーソース間に基準電流源からの基準電流が流れるように、ＴＦＴＴ２３の電流能力に合わせてそのゲート電圧が設定される。

【０１３０】安定状態になった後に、信号ＭＳＷ＿１がロウレベルになると共に、第２段目のＦ／Ｆの出力信号ＭＳＷ＿２がハイレベルになると、Ｆ／Ｆ２９０＿１が設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｃ内の１出力Ｄ／Ｉ変換部２３０ｃのスイッチＳＷ２３ａ及びＳＷ２３ｂがオフになる。この時、Ｆ／Ｆ２９０＿１が設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｃ内の１出力Ｄ／Ｉ変換部２３０ｃの容量素子Ｃ２によって、ＴＦＴＴ２３が基準電流を流すような電圧が保持される。容量素子Ｃ２の一端は、出力用ＴＦＴＴ２０乃至Ｔ２２のゲートに接続されているので、出力用ＴＦＴＴ２０乃至Ｔ２２は、ＴＦＴＴ２３に対する夫々の電流能力比に対応して、夫々１階調目に対応する電流、２階調目に対応する電流、４階調目に対応する電流を流すことができる。このような、信号ＭＳＷがハイレベルとなっている期間を、そのＲＧＢ　Ｄ／Ｉ変換部２２０ｃにおける３出力電流記憶期間とする。一方、第２段目のＦ／Ｆが設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｃ内のスイッチＳＷ２３ａ及びＳＷ２３ｂはオンとなり、安定した状態では、ＴＦＴＴ２３のドレインーソース間に基準電流が流れるように飽

和領域で動作し、その基準電流が流れるように、ＴＦＴＴ２３の電流能力に合わせてゲート電圧が設定される。

【０１３１】電流記憶期間では、上述のような３出力電流記憶期間が、全てのＲＧＢ　Ｄ／Ｉ変換部２２０ｃについて繰り返され、全ての１出力Ｄ／Ｉ変換部２３０ｃに基準電流が記憶される。

【０１３２】電流駆動期間（第１の動作期間）においては、垂直走査回路３００が１行ずつ制御線を選択していく。

【０１３３】走査パルスＹ＿１がハイレベルになると、第１行目の制御線が選択され、これに同期して出力数分の第１行目の３ビットデジタル階調データＤ０乃至Ｄ２が出力毎に１出力Ｄ／Ｉ変換部２３０ｃに入力される。デジタル階調データＤ０乃至Ｄ２が入力されると、これらのレベル（ハイレベル（Ｈ）／ロウレベル（Ｌ））に応じてスイッチＳＷ２０乃至ＳＷ２２のオン／オフが制御され、直前のフレームの電流駆動期間で記憶されていた電流が各ＴＦＴＴ２０乃至Ｔ２２の電流能力に応じて出力される。この結果、表１に示すような階調表現が可能となる。従って、出力電流値は、０から７×ｉ０まで、入力されるデジタル階調データによって、調整することができる。また、電流記憶期間（第２の動作期間）で電流能力のばらつきに合わせて基準電流を記憶し、近接領域では電流能力のばらつきが小さいとしているので、大きな領域での電流能力ばらつきに関係なく、電流ばらつきは小さく、高い精度が得られる。

【０１３４】一方、電流駆動期間（第１の動作期間）では、シフトレジスタは動作せず、全てのスイッチＳＷ２３ａ及びＳＷ２３ｂは常にオフのままである。

【０１３５】そして、以上のような動作を各フレームについて繰り返すことにより、表示部４００において階調データＤ０乃至Ｄ２に応じた表示が行われ、その際、高精度な電流が画素回路に供給される。

【０１３６】このような第１３の実施例によれば、基準電流が第１の実施例における基準電流の最低値の４倍であるため、基準電流を流す配線の負荷の充放電を高速に行うことができ、素早く安定状態にすることができる。従って、電流記憶期間を短縮して電流駆動期間を長くすることができるため、より一層精度の高い電流を表示部内の画素に供給することができる。

【０１３７】なお、第１３の実施例に対して、第２乃至第１２の実施例のように、画素回路が図３８（ｂ）に示すような構成の場合にトランジスタの極性を変えてもよく、スイッチとしてトランジスタを使用してもよく、スイッチＳＷ２３ａ及びＳＷ２３ｂのオフのタイミングを互いにずらすことやトランジスタを追加することで出力電流精度を上げてもよい。更に、例えばＴＦＴＴ２３の電流能力をＴＦＴＴ２２の電流能力よりも大きくすることで、基準電流の最低値をより大きくすることができる。この場合、電流記憶期間を短縮し、電流駆動期間を長くすることができるため、表示部内の画素への配線が持つ負荷等の充放電時間をより長く確保することができるようになり、より一層高い精度の電流を画素に供給することができる。

【０１３８】次に、本発明の第１４の実施例について説明する。第１４の実施例は、第１３の実施例における１出力Ｄ／Ｉ変換部の構成を変更したものであり、例えば図３８（ａ）に示す画素回路に対して適用されるものであり、近接領域の電流能力ばらつきがやや小さい場合に使用することができる。図２１は本発明の第１４の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【０１３９】第１４の実施例における１出力Ｄ／Ｉ変換部２３０ｄにおいては、ＴＦＴＴ２３が設けられておらず、スイッチＳＷ２３ａの一端がＴＦＴＴ２２のドレインに接続されている。また、スイッチＳＷ２３ｂはＴＦＴＴ２２のドレインとソースとの間に接続されている。

【０１４０】なお、第１３の実施例と同様に、基準電流の電流値は、発光色が赤、青、緑である夫々の電流輝度特性に合わせており、基準電流ＩＲ２の電流値ｉｒ２は発光色が赤の４階調目に対応し、基準電流ＩＧ２の電流値ｉｇ２は発光色が緑の４階調目に対応し、基準電流ＩＢ２の電流値ｉｂ２は、発光色が青の４階調目に対応している。つまり、赤（Ｒ）表示用の１出力Ｄ／Ｉ変換部２３０ｄに供給される基準電流は赤表示用の発光素子の４階調目の輝度に対応する基準電流ＩＲ２である。但し、発光素子の電流－輝度特性が比例関係を有するので、１階調目に対応する電流値をｉｒ０とすると、ｉｒ２＝４×ｉｒ０となる。同様に、緑（Ｇ）表示用又は青（Ｂ）表示用の１出力Ｄ／Ｉ変換部２３０ｃには、夫々基準電流ＩＧ２又はＩＢ２が入力される。従って、本実施例では、入力される基準電流の最小値は、第１の実施例の４倍となる。なお、基準電流を４階調目に対応させた理由は、後述のように、１出力Ｄ／Ｉ変換部２３０ｄの出力用ＴＦＴＴ２０、Ｔ２１の電流能力と電流を記憶・出力するＴＦＴＴ２２の電流能力とを１：２：４になるように設計したためである。

【０１４１】このように構成された第１４の実施例に係る発光表示装置用半導体装置も、第１の実施例と同様に、図４に示すタイミングチャートに基づいて動作する。

【０１４２】第１４の実施例における電流記憶期間（第２の動作期間）において、各１出力Ｄ／Ｉ変換部２３０ｄは夫々に基準電流源から供給された基準電流（ＩＲ２、ＩＧ２又はＩＢ２のいずれか）を記憶する。ここで、本期間においては、全デジタル階調データをロウレベルとし、１出力Ｄ／Ｉ変換部２３０ｄのスイッチＳＷ２０乃至ＳＷ２２は、オフである。

【０１４３】電流記憶期間の開始と共に、スタート信号ＩＳＴとしてパルス信号が第１段目のＦ／Ｆ２９０＿１

に入力され、このパルス信号の入力と同時に、クロック信号ＩＣＬ及びクロック反転信号ＩＣＬＢがＦ／Ｆ２９０＿１に入力されることで、ｎ個のＦ／Ｆ２９０から構成されるシフトレジスタが動作し始める。第１段目のＦ／Ｆ２９０＿１の出力信号ＭＳＷ＿１がハイレベルになると、このＦ／Ｆ２９０＿１が設けられているＲＧＢ　Ｄ／Ｉ変換部２２０ｃ内の１出力Ｄ／Ｉ変換部２３０ｄに設けられているスイッチＳＷ２３ａ及びＳＷ２３ｂがオンとなる。スイッチＳＷ２３ａ及びＳＷ２３ｂがオンとなると、１出力Ｄ／Ｉ変換部２３０ｄの電流記憶・出力用ＴＦＴＴ２２は、そのゲートードレイン間がショートされるため、飽和領域で動作する。その後、安定状態になると、ＴＦＴＴ２２のドレインーソース間に基準電流源からの基準電流が流れるように、ＴＦＴＴ２２の電流能力に合わせてそのゲート電圧が設定される。

【０１４４】安定状態になった後に、信号ＭＳＷ＿１がロウレベルになると共に、第２段目のＦ／Ｆの出力信号ＭＳＷ＿２がハイレベルになると、Ｆ／Ｆ２９０＿１が設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｃ内の１出力Ｄ／Ｉ変換部２３０ｄのスイッチＳＷ２３ａ及びＳＷ２３ｂがオフになる。この時、Ｆ／Ｆ２９０＿１が設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｃ内の１出力Ｄ／Ｉ変換部２３０ｄの容量素子Ｃ２によって、ＴＦＴＴ２２が基準電流を流すような電圧が保持される。容量素子Ｃ２の一端は、出力用ＴＦＴＴ２０及びＴ２１のゲートに接続されているので、出力用ＴＦＴＴ２０乃至Ｔ２２は、夫々の電流能力比に対応して、１階調目に対応する電流、２階調目に対応する電流、４階調目に対応する電流を流すことができる。このような、信号ＭＳＷがハイレベルとなっている期間を、そのＲＧＢＤ／Ｉ変換部２２０ｃにおける３出力電流記憶期間とする。一方、第２段目のＦ／Ｆが設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｃ内のスイッチＳＷ２３ａ及びＳＷ２３ｂはオンとなり、安定した状態では、ＴＦＴＴ２２のドレインーソース間に基準電流が流れるように飽和領域で動作し、その基準電流が流れるように、ＴＦＴＴ２２の電流能力に合わせてゲート電圧が設定される。

【０１４５】電流記憶期間では、上述のような３出力電流記憶期間が、全てのＲＧＢ　Ｄ／Ｉ変換部２２０ｃについて繰り返され、全ての１出力Ｄ／Ｉ変換部２３０ｄに基準電流が記憶される。

【０１４６】電流駆動期間（第１の動作期間）においては、垂直走査回路３００が１行ずつ制御線を選択していく。

【０１４７】走査パルスＹ＿１がハイレベルになると、第１行目の制御線が選択され、これに同期して出力数分の第１行目の３ビットデジタル階調データＤ０乃至Ｄ２が出力毎に１出力Ｄ／Ｉ変換部２３０ｄに入力される。デジタル階調データＤ０乃至Ｄ２が入力されると、これらのレベル（ハイレベル（Ｈ）／ロウレベル（Ｌ））に応じてスイッチＳＷ２０乃至ＳＷ２２のオン／オフが制御され、直前のフレームの電流駆動期間で記憶されていた電流が各ＴＦＴＴ２０乃至Ｔ２２の電流能力に応じて出力される。この結果、表１に示すような階調表現が可能となる。従って、出力電流値は、０から７×ｉ０まで、入力されるデジタル階調データによって、調整することができる。また、電流記憶期間（第２の動作期間）で４階調目に対応する基準電流をＴＦＴＴ２電流能力ばらつきに合わせて記憶し、ＴＦＴＴ２２にて４階調目に対応する電流を出力しているため、４階調目に対応する電流として高い精度の電流を出力できる。更に、ＴＦＴＴ２０及びＴ２１にて出力する電流は、夫々１階調目、２階調目に対応するものであるが、これらの電流値は、４階調目の電流の半分以下であり、電流能力ばらつきによって電流値が変動しても、その影響は、４階調目がばらついた場合と比較すれば小さい。従って、近接領域に電流ばらつきがいくらかある場合でも、精度の高い電流を供給することができる。

【０１４８】一方、電流駆動期間（第１の動作期間）では、シフトレジスタは動作せず、全てのスイッチＳＷ２３ａ及びＳＷ２３ｂは常にオフのままである。

【０１４９】そして、以上のような動作を各フレームについて繰り返すことにより、表示部４００において階調データＤ０乃至Ｄ２に応じた表示が行われ、その際、高精度な電流が画素回路に供給される。

【０１５０】このような第１４の実施例によれば、基準電流が第１の実施例における基準電流の最低値の４倍であるため、基準電流を流す配線の負荷の充放電を高速に行うことができ、素早く安定状態にすることができる。従って、電流記憶期間を短縮して電流駆動期間を長くすることができるため、表示部内の画素への配線が持つ負荷等の充放電時間を長く確保することが可能である。このため、より一層高い精度の電流を画素に供給することができる。

【０１５１】なお、第１４の実施例に対して、第２乃至第１０の実施例のように、画素回路が図３８（ｂ）に示すような構成の場合にトランジスタの極性を変えてもよく、スイッチとしてトランジスタを使用してもよく、スイッチＳＷ２３ａ及びＳＷ２３ｂのオフのタイミングを互いにずらすことやトランジスタを追加することで出力電流精度を上げてもよい。更に、ＴＦＴＴ２２のみ電流を記憶・出力するトランジスタとするのではなく、ＴＦＴＴ２１をも電流を記憶・出力するようにし、基準電流を増やすことで、更に近接領域がばらついた場合でも、より高い精度の電流を供給することができるようになる。また、例えば、第１３又は第１４の実施例の発光表示装置用半導体装置において、第１３又は１４の実施例の１出力Ｄ／Ｉ変換回路に第１乃至１２の実施例の１ビットＤ／Ｉ変換回路を１又は複数追加することで、１又は複数ビット分の精度を高めることが可能となる。

【０１５２】次に、本発明の第１５の実施例について説明する。第１５の実施例は、例えば図３８（ａ）に示す画素回路に対して適用されるものである。図２２は本発明の第１５の実施例に係る発光表示装置用半導体装置の構成を示すブロック図である。

【０１５３】第１５の実施例には、Ｄ／Ｉ変換部２１０ｄが設けられており、このＤ／Ｉ変換部２１０ｄに、発光表示装置への出力数（３×ｎ）分の１出力Ｄ／Ｉ変換部２３０ｅ、及び３出力毎に設けられたｎ個のフリップフロップ（Ｆ／Ｆ）２９０ｃ＿１乃至２９０ｃ＿ｎから構成されたシフトレジスタが設けられている。シフトレジスタには、電流を記憶するタイミング制御のためのスタート信号ＩＳＴ、クロック信号ＩＣＬ、このクロック信号ＩＣＬの反転信号ＩＣＬＢ及び電流セレクタ信号ＩＳＥＬ１が入力される。また、１出力Ｄ／Ｉ変換部２３０ｅには、各出力のデジタル画像データＤ０乃至Ｄ２が入力され、参照するための基準電流ＩＲ０乃至ＩＲ２、ＩＧ０乃至ＩＧ２、ＩＢ０乃至ＩＢ２のいずれかがそれに割り当てられた発光色に応じて入力される。基準電流は、発光色が赤、青、緑である夫々の発光素子の電流－輝度特性にあった電流値であり、基準電流ＩＲ０の電流値ｉｒ０は発光色が赤の発光素子の１階調目に対応し、基準電流ＩＲ１の電流値ｉｒ１は発光色が赤の発光素子の２階調目に対応し、基準電流ＩＲ２の電流値ｉｒ２は発光色が赤の４階調目に対応する。同様に、基準電流ＩＧ０乃至ＩＧ２の電流値は、夫々発光色が緑の１階調目、２階調目、４階調目に対応し、基準電流ＩＢ０乃至ＩＢ２は、夫々発光色が青の１階調目、２階調目、４階調目に対応する。また、１出力Ｄ／Ｉ変換部２３０ｅには、電流セレクタ信号ＩＳＥＬ１及びＩＳＥＬ２が入力される。１個のＦ／Ｆ２９０ｃと、このＦ／Ｆ２９０ｃから出力された信号ＭＳＷＡ及びＭＳＷＢが入力される３個の１出力Ｄ／Ｉ変換部２３０ｅとから１個のＲＧＢ　Ｄ／Ｉ変換部２２０ｄが構成されている。

【０１５４】図２３は１出力Ｄ／Ｉ変換部２３０ｅの構成を示すブロック図である。１出力Ｄ／Ｉ変換部２３０ｅは、夫々３個の１ビットＤ／Ｉ変換部２３１により構成される出力ブロック２４０ａ及び２４０ｂ並びにデータ作成回路２３２が設けられている。また、夫々電流セレクタ信号ＩＳＥＬ１及びＩＳＥＬ２により制御され、出力ブロック２４０ａ及び２４０ｂのうち、どちらのブロックから電流を出力するかを選択するスイッチＳＷ３１、ＳＷ３２が設けられている。データ作成回路２３２は、１出力分のデジタル階調データＤ０乃至Ｄ２並びに電流セレクタ信号ＩＳＥＬ１及びＩＳＥＬ２に基づいて、データ信号Ｄ０Ａ乃至Ｄ２Ａ及びＤ０Ｂ乃至Ｄ２Ｂを生成する。データ信号Ｄ０Ａ乃至Ｄ２Ａは出力ブロック２４０ａに入力され、データ信号Ｄ０Ｂ乃至Ｄ２Ｂは出力ブロック２４０－2に入力される。また、出力ブロック２４０ａには、Ｆ／Ｆ２９０ｃの出力信号ＭＳＷＡが入力され、出力ブロック２４０ｂには、Ｆ／Ｆ２９０ｃの出力信号ＭＳＷＢが入力される。また、出力ブロック２４０ａ及び２４０ｂには、参照するための基準電流Ｉ０乃至Ｉ２が入力される。なお、１ビットＤ／Ｉ変換部２３１は、第１の実施例のものと同様の構成を有しており、発光素子の電流－輝度特性が比例関係を有するので、ｉｒ１＝２×ｉｒ０及びｉｒ２＝４×ｉｒ０の関係が成り立つ。同様に、緑（Ｇ）表示用又は青（Ｂ）表示用の１出力Ｄ／Ｉ変換部２３０に設けられている１ビットＤ／Ｉ変換部２３１であって、階調データＤ０、Ｄ１、Ｄ２が入力されるものには、夫々基準電流ＩＧ０又はＩＢ０、基準電流ＩＧ１又はＩＢ１、基準電流ＩＧ２又はＩＢ２が入力される。

【０１５５】図２４はデータ作成回路２３２の一例の構成を示す回路図である。データ作成回路２３２には、例えば電流セレクタ信号ＩＳＥＬ１を１入力とするナンドゲートＮＡＮＤ０Ａ乃至ＮＡＮＤ２Ａ、夫々これらの出力を反転するインバータＩＶ０Ａ乃至ＩＶ２Ａ、電流セレクタ信号ＩＳＥＬ２を１入力とするナンドゲートＮＡＮＤ０Ｂ乃至ＮＡＮＤ２Ｂ、夫々これらの出力を反転するインバータＩＶ０Ｂ乃至ＩＶ２Ｂが設けられている。ナンドゲートＮＡＮＤ０Ａ及びＮＡＮＤ０Ｂには、階調データＤ０が更に入力され、ナンドゲートＮＡＮＤ１Ａ及びＮＡＮＤ１Ｂには、階調データＤ１が更に入力され、ナンドゲートＮＡＮＤ２Ａ及びＮＡＮＤ２Ｂには、階調データＤ２が更に入力される。そして、インバータＩＶ０Ａ乃至ＩＶ２Ａ及びＩＶ０Ｂ乃至ＩＶ２Ｂから、夫々データ信号Ｄ０Ａ乃至Ｄ２Ａ及びＤ０Ｂ乃至Ｄ２Ｂが出力される。但し、この構成は一例であり、同様の信号を出力できれば、他の構成をとってもよい。

【０１５６】次に、上述のように構成された第１５の実施例に係る発光表示装置用半導体装置の動作について説明する。図２５は本発明の第１５の実施例に係る発光表示装置用半導体装置の動作を示すタイミングチャートである。

【０１５７】表示部４００（図３５参照）を垂直走査し始めてから、次の垂直走査が始まるまでを１フレームとする。本実施例の場合、互いに排他的な電流セレクタ信号ＩＳＥＬ１及びＩＳＥＬ２の一方がハイレベルになる２種類のフレームが交互に現れる。

【０１５８】先ず、第１のフレームについて説明する。第１のフレームでは、電流セレクタ信号ＩＳＥＬ１がハイレベル、電流セレクタ信号ＩＳＥＬ２がロウレベルになる。この場合、出力ブロック２４０ａ及び２４０ｂにおいて、デジタル画像データＤＡ０乃至ＤＡ２が入力される第１の出力ブロック２４０ａでは、スイッチＳＷ１がオンし、電流を出力する。一方、デジタル画像データＤＢ０乃至ＤＢ２が入力される第２の出力ブロック２４０ｂでは、スイッチＳＷ２がオフし、電流を記憶する。より詳細には、出力ブロック２４０ｂ内の１ビットＤ／

Ｉ変換部２３１が、基準電流ＩＲ０乃至ＩＲ２、ＩＧ０乃至ＩＧ２、ＩＢ０乃至ＩＢ２のいずれか１つを記憶する。但し、本フレームにおいて、デジタル階調データＤＢ０乃至ＤＢ２はロウレベルにあり、出力ブロック２４０ｂ内の１ビットＤ／Ｉ変換部２３１のスイッチＳＷ１はオフとなっている。

【０１５９】次に、出力ブロック２４０ｂの電流を記憶する動作について説明する。

【０１６０】第１のフレームの開始と共に、スタート信号ＩＳＴとしてパルス信号が第１段目のＦ／Ｆ２９０ｃ＿１に入力され、このパルス信号の入力と同時に、クロック信号ＩＣＬ及びクロック反転信号ＩＣＬＢがＦ／Ｆ２９０ｃ＿１に入力されることで、ｎ個のＦ／Ｆ２９０から構成されるシフトレジスタが動作し始める。第１段目のＦ／Ｆ２９０ｃ＿１の出力信号ＭＳＷＢ＿１がハイレベルになると、この出力信号ＭＳＷＢ＿１が入力される１出力Ｄ／Ｉ変換部２３０ｅに設けられた出力ブロック２４０ｂの各１ビットＤ／Ｉ変換部２３１のスイッチＳＷ２及びＳＷ３がオンとなる。スイッチＳＷ２及びＳＷ３がオンになると、その１ビットＤ／Ｉ変換部２３１内の電流記憶・出力用ＴＦＴＴ１は、そのゲートードレイン間がショートされるため、飽和領域で動作する。そして、本動作が安定した状態では、ＴＦＴＴ１のドレインーソース間に基準電流が流れるように、ＴＦＴＴ１の電流能力に合わせてそのゲート電圧が設定される。

【０１６１】安定状態になった後に、信号ＭＳＷＢ＿１がロウレベルになると共に、第２段目のＦ／Ｆの出力信号ＭＳＷＢ＿２がハイレベルになると、Ｆ／Ｆ２９０＿１が設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｄ内の１出力Ｄ／Ｉ変換部２３０ｅに設けられた出力ブロック２４０ｂ内のスイッチＳＷ２及びＳＷ３がオフとなる。この時、Ｆ／Ｆ２９０＿１が設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｄ内の出力ブロック２４０ｂのＴＦＴＴ１のゲート電圧は、容量素子Ｃ１によって基準電流が流れるような電圧に保持される。この結果、ＴＦＴＴ１には、夫々の電流能力に関わらず、基準電流が記憶される。このような、信号ＭＳＷがハイレベルとなっている期間を、そのＲＧＢ　Ｄ／Ｉ変換部２２０ｄにおける３出力電流記憶期間とする。一方、第２段目のＦ／Ｆが設けられたＲＧＢ　Ｄ／Ｉ変換部２２０ｄ内の出力ブロック２４０ｂのスイッチＳＷ２及びＳＷ３はオンとなり、安定した状態では、その１ビットＤ／Ｉ変換部２３１のＴＦＴＴ１のドレインーソース間に基準電流が流れるように飽和領域で動作し、その基準電流が流れるように、ＴＦＴＴ１の電流能力に合わせてゲート電圧が設定される。

【０１６２】第１のフレーム期間では、上述のような３出力電流記憶期間が、全てのＲＧＢＤ／Ｉ変換部２２０ｄ内の第２の出力ブロック２４０ｂについて繰り返され、全ての１出力Ｄ／Ｉ変換部２３０ｅの第２の出力ブロック２４０ｂに基準電流が記憶される。

【０１６３】次に、第１のフレームにおける第１の出力ブロック２４０ａの動作について説明する。第１のフレームで、垂直走査回路３００が１行ずつ制御線を選択していく。図２５には、第１行目、第２行目の出力である走査パルスＹ＿１、Ｙ＿２を示している。

【０１６４】走査パルスＹ＿１がハイレベルになると、第１行目の制御線が選択され、これに同期して出力数分の第１行目の３ビットデジタル階調データＤ０乃至Ｄ２が出力毎に１出力Ｄ／Ｉ変換部２３０ｅ内の第１の出力ブロック２４０ａに入力される。デジタル階調データＤ０乃至Ｄ２が入力されると、これらのレベル（ハイレベル（Ｈ）／ロウレベル（Ｌ））に応じて１ビットＤ／Ｉ変換部２３１内のスイッチＳＷ１のオン／オフが制御され、直前のフレームの電流駆動期間でＴＦＴＴ１に記憶されていた電流が出力され、階調表現が行われる。

【０１６５】表１に示すように、出力電流値は、０から７×ｉ０まで、入力されるデジタル階調データによって、調整することができる。また、直前のフレームでＴＦＴＴ１の電流能力に合わせて、基準電流源と同等な電流が流れるようにゲート電圧が設定され、同じＴＦＴＴ１を使用して出力しているため、電流能力ばらつきに関係なく、出力電流のばらつきは小さく、高い精度が得られる。

【０１６６】一方、第１のフレームでは、シフトレジスタの出力ＭＳＷＡは、常にロウレベルであり、全ての出力ブロック２４０ａ内のスイッチＳＷ２及びＳＷ３は常にオフのままである。

【０１６７】次の第２のフレームでは、電流セレクタ信号ＩＳＥＬ１をロウレベル、電流セレクタ信号ＩＳＥＬ２をハイレベルとすることで、第１の出力ブロック２４０ａの動作と、第２の出力ブロック２４０ｂの動作とを入れ替える。この結果、第１の出力ブロック２４０ａは電流を記憶し、第２の出力ブロック２４０ｂは電流を出力する。

【０１６８】２フレーム毎に以上の動作を繰り返すことにより、本実施例は、高精度な電流を画素回路に供給することができる。更に、本実施例では、１出力に２個の出力ブロックが設けられているので、各フレームにおいて、一方の出力ブロックを電流を出力するために使用し、他方の出力ブロックは電流を記憶するために使用することができ、電流記憶期間を別に設ける必要がない。これにより、１フレーム期間がすべて電流駆動期間となり、表示部内の画素への配線が持つ負荷等の充放電時間を長く確保することが可能となる。従って、より一層高い精度の電流を画素に供給することができる。

【０１６９】なお、第１５の実施例に対して、第２乃至第１４の実施例を適用してもよく、同様な効果を得ることができる。

【０１７０】また、電流記憶の周期は、１フレーム毎に限定されるものではなく、数フレーム毎となっていても

よい。電流記憶の周期を数フレーム毎にすることにより、電流記憶の期間が長くなるため、より一層高い精度で電流を記憶することができるようになる。但し、記憶時の電流に対応するゲート電圧に、トランジスタのリーク等により求められる精度以下の変動が生じないことが必要とされる。

【０１７１】次に、本発明の第１６の実施例について説明する。第１６の実施例は、１出力Ｄ／Ｉ変換部の後段にプリチャージ回路を設けたものである。図２６は本発明の第１６の実施例に係る発光表示装置用半導体装置の構成を示すブロック図である。

【０１７２】第１６の実施例には、Ｄ／Ｉ変換部２１０ｅが設けられている。Ｄ／Ｉ変換部２１０ｅは、各１出力Ｄ／Ｉ変換部２３０ｅの後段に、夫々プリチャージ回路２５０が設けられている点を除いて、第１６の実施例におけるＤ／Ｉ変換部２１０ｄと同様の構成を有している。プリチャージ回路２５０には、プリチャージ信号ＰＣ入力される。

【０１７３】プリチャージ回路２５０は、プリチャージ信号により設定される期間に、Ｄ／Ｉ変換部２１０ｄの各出力おいて、１出力Ｄ／Ｉ変換部２３０ｅの出力電流の代わりに、その１出力Ｄ／Ｉ変換部の出力電流により決まる電圧を出力する。図２７はプリチャージ回路２５０の構成例を示す回路図である。プリチャージ回路２５０には、プリチャージ信号ＰＣにより制御されるＮチャネルトランジスタＴ３１乃至Ｔ３３及びＰチャネルトランジスタＴ３４が設けられている。トランジスタＴ３１及びＴ３２の一端には、１出力Ｄ／Ｉ変換部２３０ｅからの出力電流ＩＯＵＴが入力され、トランジスタＴ３１の他端には、擬似負荷回路２５２及びオペアンプ２５１の非反転入力端子が接続されている。擬似附加回路２５２において、トランジスタＴ３３の一端がトランジスタＴ３１に接続され、トランジスタＴ３３の他端にＰチャネルトランジスタＴ３５のゲートが接続されている。トランジスタＴ３５のソースには電圧ＶＥＬが供給され、他端はトランジスタＴ３１に接続されている。オペアンプ２５１の反転入力端子には、オペアンプ２５１自体の出力信号が入力され、トランジスタＴ３２の一端は、オペアンプ２５１の出力端子に接続され、他端はトランジスタＴ３４の他端に接続されている。トランジスタＴ３２及びＴ３４の共通接続点から発光素子の駆動電流が出力される。

【０１７４】このようなプリチャージ回路２５０においては、トランジスタＴ３４により、１出力Ｄ／Ｉ変換部２３０ｅの出力電流ＩＯＵＴを出力電流Ｉｏｕｔとして直接出力するか、擬似負荷回路２５２に出力するかが決定される。また、トランジスタＴ３２により、オペアンプ２５１の出力をＤ／Ｉ変換部２１０ｅの出力とするかどうかが決定される。更に、オペアンプ２５１は、その出力を反転入力に負帰還しているため、非反転入力に入力される電圧をボルテージフォロワ出力する。また、トランジスタＴ３５は、表示部４００内の画素回路（図３８（ａ））のＴＦＴＴ１０２と同じトランジスタ、又は同等の電流能力を有するトランジスタである。但し、擬似負荷回路２５２としては、トランジスタＴ３５のゲートドレイン間を短絡し、トランジスタＴ３３を設けない構成としてもよい。また、トランジスタＴ３１、Ｔ３２及びＴ３４は、スイッチとして作用するため、例えばプリチャージ信号ＰＣの極性によっては、逆の極性のトランジスタとすることもでき、また、プリチャージ信号ＰＣ自体及びその反転信号を入力する構成とすれば、どのような極性のトランジスタを使用することも可能である。

【０１７５】次に、プリチャージ回路２５０の動作について説明する。図２８はプリチャージ回路２５０の動作を示すタイミングチャートである。

【０１７６】本実施例においては、１ライン選択期間がプリチャージ信号ＰＣのレベルにより、第１の期間と第２の期間とに分けられる。

【０１７７】第１の期間では、プリチャージ信号ＰＣがハイレベルとなっており、プリチャージ期間である。走査パルスＹ＿１がハイレベルになると、第１行目の制御線が選択され、これに同期して出力数分の第１行目の３ビットデジタル階調データＤ０乃至Ｄ２が出力毎に１出力Ｄ／Ｉ変換部２３０ｅに入力される。１出力Ｄ／Ｉ変換部２３０ｅは、入力されたデジタル階調データＤＡ０乃至ＤＡ２から表１に示す関係に従って電流を出力する。この時、プリチャージ信号ＰＣがハイベルとなっていれば、プリチャージ回路２５０内のトランジスタＴ３４がオフ、トランジスタＴ３１及びＴ３２がオンとなる。よって、プリチャージ回路２５０において、１出力Ｄ／Ｉ変換部２３０ｅの出力電流が擬似負荷回路２５２に流れる。擬似負荷回路２５２には、トランジスタＴ３５が設けられているため、出力電流Ｉｏｕｔが安定して流れた場合、トランジスタＴ３５のゲート電圧は出力電流Ｉｏｕｔが表示部内の画素回路に安定して流れた場合のゲート電圧とほぼ同じ電圧となる。そして、この電圧は、オペアンプ２５２により構成されたボルテージフォロワの入力となり、このプリチャージ期間ではトランジスタＴ３２がオンとなっているため、ボルテージフォロワの出力がＤ／Ｉ変換部２１０ｅの出力となる。よって、本期間において、表示部内の画素回路にトランジスタＴ３５のゲート電圧を印加することができる。

【０１７８】擬似負荷回路２５２は、画素回路よりも１出力Ｄ／Ｉ変換部２３０ｅの近くにあり、充放電する必要がある配線負荷等が極めて小さいため、１出力Ｄ／Ｉ変換部２３０ｅの一定出力電流をトランジスタＴ３５に安定して流すという動作は、１出力Ｄ／Ｉ変換回路の一定出力電流で表示部内の画素回路を駆動する場合と比較すると、出力電流値が低い場合でも、非常に高速に行う

ことができる。また、トランジスタＴ３５のゲート電圧を表示部内の画素回路に印加するという動作も、ボルテージフォロワという低インピーダンスの出力にて行われるため、高速に実現できる。

【０１７９】第２の期間は、プリチャージ信号ＰＣがロウレベルとなっており、電流出力期間である。プリチャージ信号ＰＣがロウレベルとなっている場合、プリチャージ回路２５０内のトランジスタＴ３４がオン、トランジスタＴ３１及びＴ３２がオフとなる。よって、プリチャージ回路２５０において、１出力Ｄ／Ｉ変換部２３０ｅの出力電流がそのまま出力され、表示部内の画素回路が駆動される。この時、第１の期間で、プリチャージ動作を行われているため、表示部内の画素回路には、１出力Ｄ／Ｉ変換部２３０ｅの出力電流が安定して流れた場合に近い電圧が印加されている。従って、第２の期間では、トランジスタＴ３５と表示部内の画素回路にあるトランジスタＴＦＴＴ１０２（図３８（ａ））の間の電流能力ばらつきを補正するという動作、及び表示部内の画素回路に出力電流Ｉｏｕｔを安定して流して駆動するという動作が行われる。この結果、第２の期間において配線負荷等を充放電する量は小さくて済む。従って、第２の期間は、プリチャージ動作を行わない場合に比べ、期間を短縮することができる。また、プリチャージ動作によって安定な電圧を出力した後、電流駆動を行うために１ライン選択期間の前の状態に影響されることなく動作が可能である。

【０１８０】その後、走査パルスＹ＿１がロウレベル、走査パルスＹ＿２がハイレベルになり、第２行目の制御線が選択され、同じ動作が繰り返される。以上の動作によって、表示部内の画素回路をより一層高い精度の電流により高速に駆動できる。

【０１８１】なお、第１６の実施例の１出力Ｄ／Ｉ変換部として第１乃至第１５の実施例を適用してもよく、また、電流を供給する回路・半導体装置が、本発明に含まれていないような場合に適用しても、同様の効果を得ることができる。

【０１８２】次に、第１７の実施例について説明する。第１７の実施例は、第１６の実施例におけるプリチャージ回路の構成を変更したものである。図２９は本発明の第１７の実施例におけるプリチャージ回路の構成を示すブロック図である。

【０１８３】第１７の実施例におけるプリチャージ回路２５０ａには、プリチャージ信号ＰＣが入力されるＮチャネルトランジスタＴ３６並びにＰチャネルトランジスタＴ３７及びＴ３８が、プリチャージ回路２５０の構成要素に加えて設けられている。トランジスタＴ３８は、オペアンプ２５１の出力端子と反転入力端子との間に接続されている。また、オペアンプ２５１の出力端子には容量素子Ｃ３が入力され、その他端と反転入力端子との間にトランジスタＴ３６が接続され、非反転入力端子との間にトランジスタＴ３７が接続されている。

【０１８４】このように構成されたプリチャージ回路２５０ａは、よく知られたオペアンプ２５１のオフセット電圧をキャンセルする回路を備え、電流駆動期間にオフセットキャンセル動作を行うことにより、オペアンプ２５１のオフセット電圧の影響を受けず、プリチャージ動作を行うことができる。他の動作は、第１６の実施例におけるプリチャージ回路２５０の動作と同様である。

【０１８５】次に、本発明の第１８の実施例を図３２に示す。第１８の実施例は、入力されるデジタルデータ信号を保持するデータレジスタ２０３と、その保持するタイミングと同期した走査信号を出力するデータシフトレジスタ２０２と、ラッチ信号に同期して全データレジスタの信号を保持し、Ｄ／Ｉ変換部２１０に出力するデータラッチ２０４と、デジタルデータ信号に従って電流を出力するＤ／Ｉ変換部２１０とを備える水平駆動回路２００である。Ｄ／Ｉ変換部２１０は、プリチャージ回路を含んでも良い。さらに、Ｄ／Ｉ変換部２１０は、本発明の第１乃至第１７のいずれかの実施例のＤ／Ｉ変換部で構成されて良い。

【０１８６】次に、本発明の第１９の実施例を図３３に示す。第１９の実施例は、第１８の実施例のＤ／Ｉ変換部２１０の出力が、セレクタ回路２１１によって、順次複数の表示部４００のデータ線に接続できるようにしたことで、回路規模を増やすことなく駆動できるデータ線、画素回路を増やすことができる。

【０１８７】次に、本発明の第２０の実施例を図３４に示す。第２０の実施例は、第１８の実施例に基準電流を作成する基準電流源２１２を水平駆動回路２００に内蔵したものである。

【０１８８】本発明の第１乃至２０の実施例では、トランジスタをＴＦＴで説明しているが、より一般的なトランジスタで構成されて良く、１つの表示部に対し、複数の水平駆動回路２００を使用しても良い。また、全てのトランジスタをＴＦＴで作成することで、表示部４００、水平駆動回路２００及び垂直走査回路３００を同じ基板上に形成してもよい。この場合、本発明の実施例におけるプリチャージ回路の負荷（回路）を表示部４００の負荷と同じ構成の負荷（回路）を作成することで、より高精度なプリチャージが実現できる。

【０１８９】また、本発明の第１乃至２０の実施例では、カラー（Ｒ、Ｇ、Ｂ）で電流－輝度特性が比例関係である発光素子を備えた発光表示装置を、夫々０階調～７階調表示の３ビットデジタル階調データが入力する４０９６色表示で駆動する実施例について説明しているが、単色の場合、又はより多ビットの場合にも、同様な構成をそのまま拡張することができる。また、トランジスタを全てＴＦＴとしているが、より一般のトランジスタでも、本発明は同様な構成により実現できる。さらに、アクティブマトリックス方式の画素回路として、図

３８（ａ）を仮定しているが、他の電流駆動方式の画素回路にも、また、単純マトリックス方式の画素に対しても、本発明は、同様な構成によって実現できる。

【０１９０】以上のような実施例は、発光表示素子を備える発光表示装置において説明しているが、より一般的な電流負荷素子を備える電流負荷デバイスに対しても適用される。

【０１９１】

【発明の効果】以上詳述したように、本発明によれば、高精度の電流を電流負荷デバイスのセル（回路）に供給することができる。これは、デジタル／電流変換装置内のトランジスタのドレインーソース間に基準電流が安定に流れる状態のゲートーソース間電圧を記憶することにより、トランジスタの電流能力ばらつきに影響を受けることなく、精度の高い電流を記憶することができ、更に電流を記憶したトランジスタにて電流を出力するためである。また、近接領域における電流能力ばらつきに従って、電流を記憶して出力するトランジスタの数を増減することもできる。記憶する電流が少なく、その電流値が大きい場合には、記憶する時間を短縮でき、出力する（駆動する）時間を延ばすことで、電流負荷デバイス内のデータ線や画素の負荷を充放電のための時間が長く確保することができる。従って、より一層高精度の電流負荷デバイスのセル（回路）に供給することができる。また、出力端子毎に電流記憶用のトランジスタ及び電流出力用のトランジスタを設け、それをフレームごとに入れ替えることで、別途に記憶期間を必要としなくなり、出力する（駆動する）時間を延ばすことができる。この結果、更に高精度の電流を電流負荷デバイスのセル（回路）に供給することができる。

【０１９２】また、デジタル／電流変換装置の出力と電流負荷デバイスとの間に、擬似負荷回路を備えたプリチャージ回路を備えることで、出力電流値が低い場合でも、電流かデバイスの画素（回路）を高速に駆動することができる。これは、出力の初期段階には、デジタル／電流変換装置の電流出力により、擬似負荷回路を高速に駆動し、擬似負荷回路から得られる電圧をボルテージフォロワにて電流負荷デバイス内のセル（回路）に供給して、ほぼデジタル／電流変換装置の電流出力が電流負荷デバイス内のセル（回路）に印加された場合の電圧を高速に印加することができ、その後、直接、デジタル／電流変換装置の電流出力にて電流負荷デバイス内のセル（回路）を駆動し、補正するという動作を行うことで、定電流による電流負荷デバイス内の画素や信号線の負荷の充放電畳を減らすことができるからである。

【図面の簡単な説明】

【図１】本発明の第１の実施例に係る電流負荷デバイス駆動用半導体装置の構成を示すブロック図である。

【図２】１出力Ｄ／Ｉ変換部２３０の構成を示すブロック図である。

【図３】１ビットＤ／Ｉ変換部２３１の構成を示すブロック図である。

【図４】本発明の第１の実施例に係る電流負荷デバイス駆動用半導体装置の動作を示すタイミングチャートである。

【図５】本発明の第２の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【図６】本発明の第３の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【図７】本発明の第４の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【図８】本発明の第５の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【図９】本発明の第６の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【図１０】本発明の第７の実施例に係る発光表示装置用半導体装置の構成を示すブロック図である。

【図１１】１出力Ｄ／Ｉ変換部２３０ａの構成を示すブロック図である。

【図１２】１ビットＤ／Ｉ変換部２３１ｆの構成を示すブロック図である。

【図１３】本発明の第７の実施例に係る電流負荷デバイス駆動用半導体装置の動作を示すタイミングチャートである。

【図１４】本発明の第８の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【図１５】本発明の第９の実施例に係る電流負荷デバイス駆動用半導体装置の構成を示すブロック図である。

【図１６】１出力Ｄ／Ｉ変換部２３０ｂの構成を示すブロック図である。

【図１７】１ビットＤ／Ｉ変換部２３１ｈの構成を示すブロック図である。

【図１８】本発明の第１０の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【図１９】本発明の第１３の実施例に係る電流負荷デバイス駆動用半導体装置の構成を示すブロック図である。

【図２０】１出力Ｄ／Ｉ変換部２３０ｃの構成を示すブロック図である。

【図２１】本発明の第１４の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。

【図２２】本発明の第１５の実施例に係る電流負荷デバイス駆動用半導体装置の構成を示すブロック図である。

【図２３】１出力Ｄ／Ｉ変換部２３０ｅの構成を示すブロック図である。

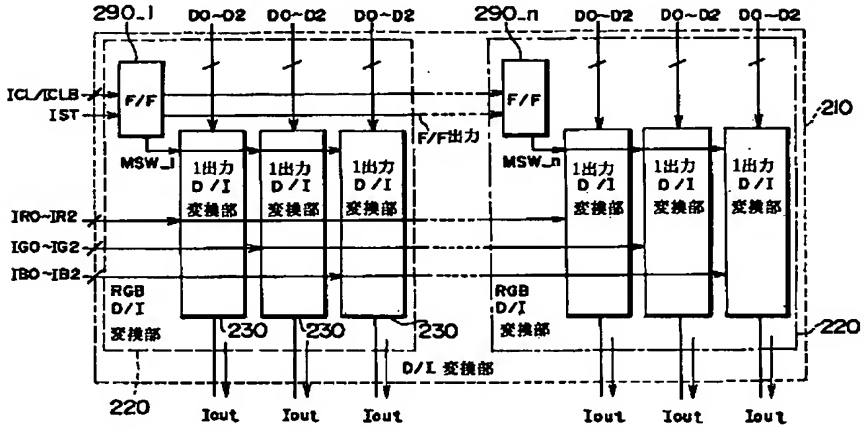
【図２４】データ作成回路２３２の一例の構成を示す回路図である。

【図２５】本発明の第１５の実施例に係る電流負荷デバイス駆動用半導体装置の動作を示すタイミングチャートである。

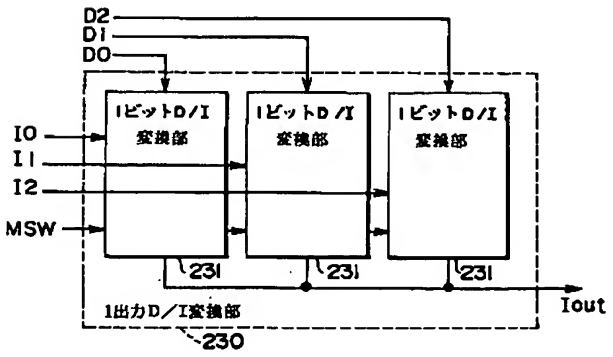
【図２６】本発明の第１６の実施例に係る電流負荷デバ

イス駆動用半導体装置の構成を示すブロック図である。
【図２７】プリチャージ回路２５０の構成を示す回路図である。
【図２８】プリチャージ回路２５０の動作を示すタイミングチャートである。
【図２９】本発明の第１７の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。
【図３０】本発明の第１１の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。
【図３１】本発明の第１２の実施例における１ビットＤ／Ｉ変換部の構成を示すブロック図である。
【図３２】本発明の第１８の実施例に係る電流負荷デバイス駆動用半導体装置の構成を示すブロック図である。
【図３３】本発明の第１９の実施例に係る電流負荷デバイス駆動用半導体装置の構成を示すブロック図である。
【図３４】本発明の第２０の実施例に係る電流負荷デバイス駆動用半導体装置の構成を示すブロック図である。
【図３５】供給される電流により輝度が決定される発光素子が各画素にある発光表示装置の構成を示す図である。
【図３６】単純マトリックス駆動の場合の１画素表示部の構成を示す回路図である。
【図３７】アクティブマトリックス駆動の場合の１画素表示部の構成を示す回路図である。
【図３８】（ａ）及び（ｂ）はアクティブマトリックス駆動の場合の１画素表示部の他の構成を示す回路図である。
【図３９】表示部４００に電流を出力するための水平駆動回路２００の構成の一例を示すブロック図である。
【図４０】１出力分のデジタル／電流変換部の第１の従来例を示す回路図である。
【図４１】１出力分のデジタル／電流変換部の第２の従来例を示す回路図である。
【符号の説明】
２１０、２１０ａ～２１０ｄ：Ｄ／Ｉ変換部
２２０、２２０ａ～２２０ｃ：ＲＧＢ　Ｄ／Ｉ変換部
２３０、２３０ａ～２３０ｃ：１出力Ｄ／Ｉ変換部（１出力Ｄ／Ｉ変換回路）
２３１、２３１ａ～２３１ｉ：１ビットＤ／Ｉ変換部（１ビットＤ／Ｉ変換回路）
２５０、２５０ａ：プリチャージ回路

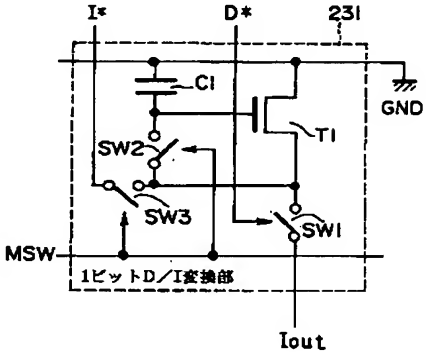
【図１】



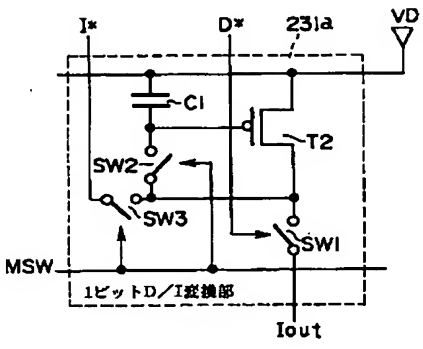
【図２】



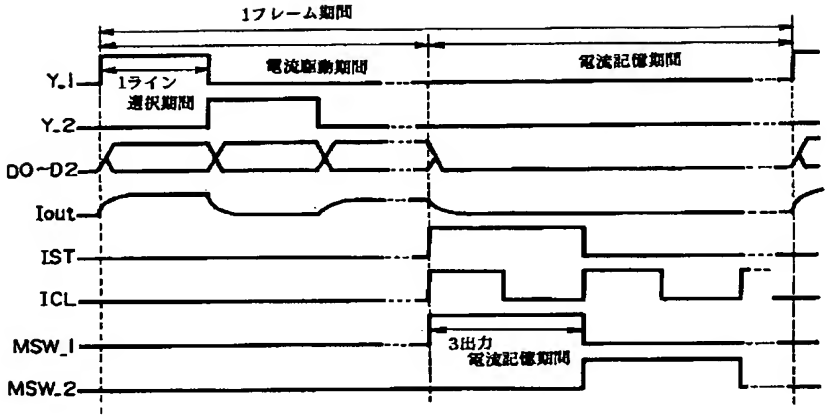
【図３】



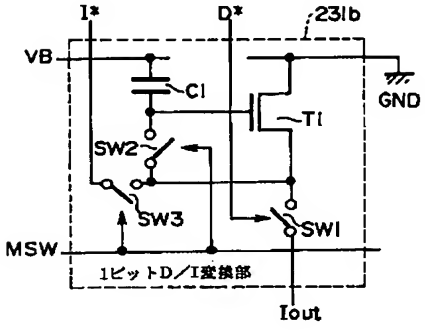
【図５】



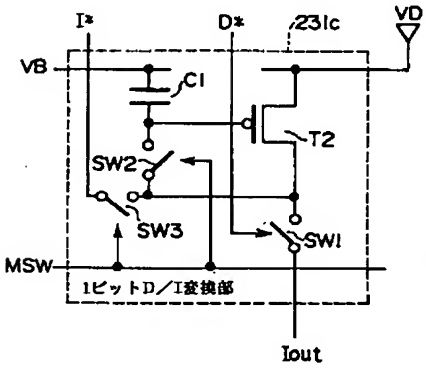
【図４】



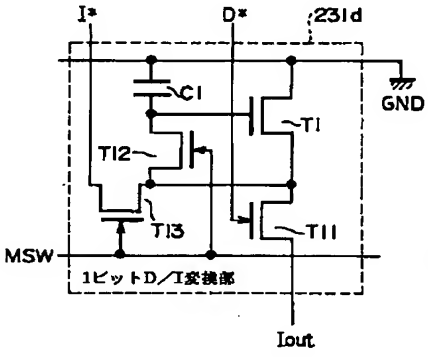
【図６】



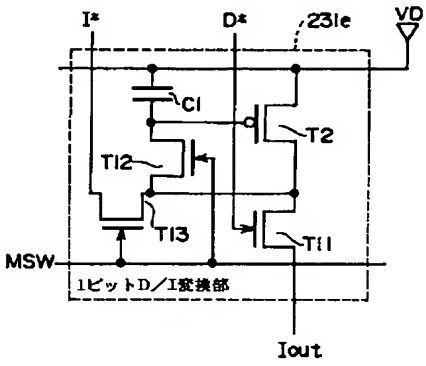
【図７】



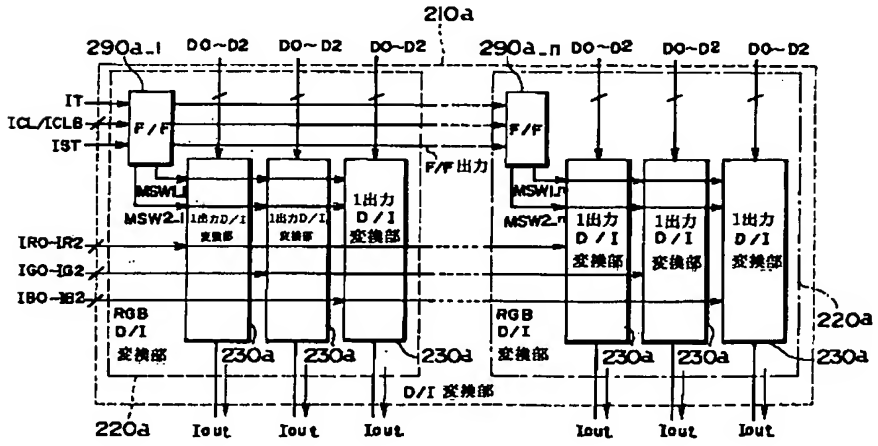
【図８】



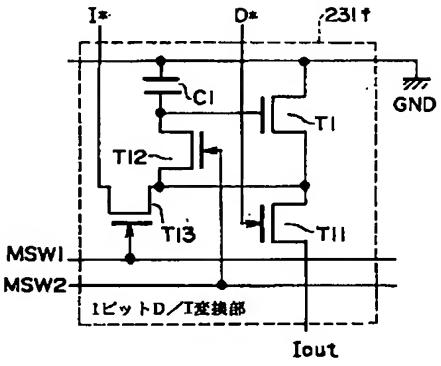
【図９】



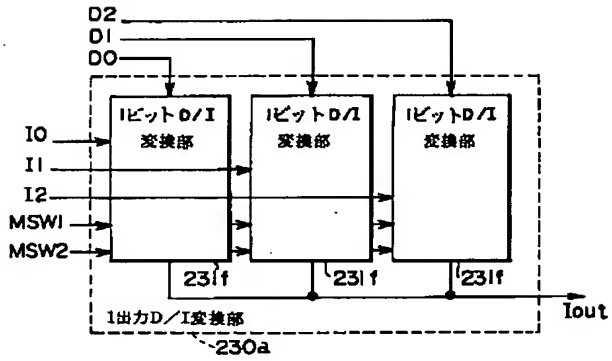
【図１０】



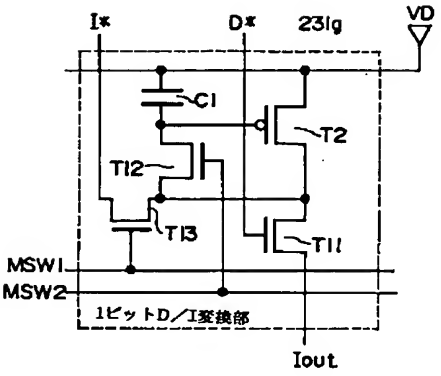
【図１２】



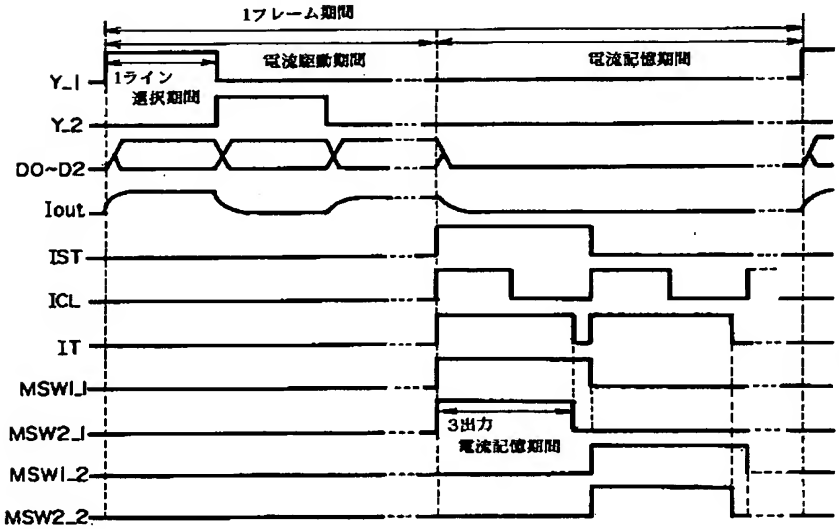
【図１１】



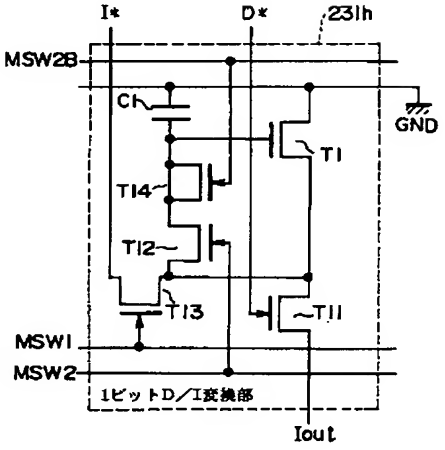
【図１４】



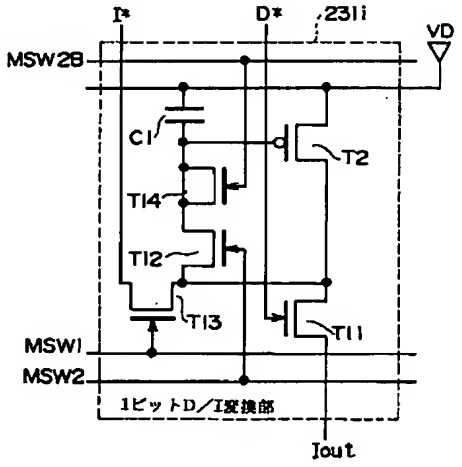
【図１３】



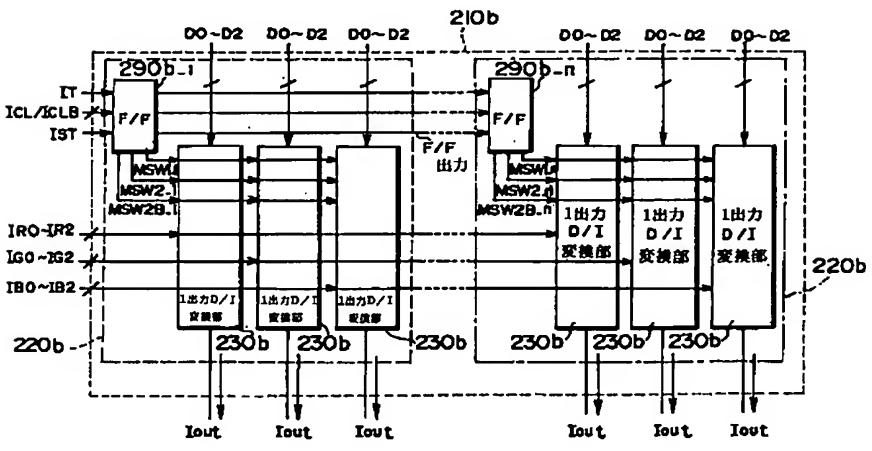
【図１７】



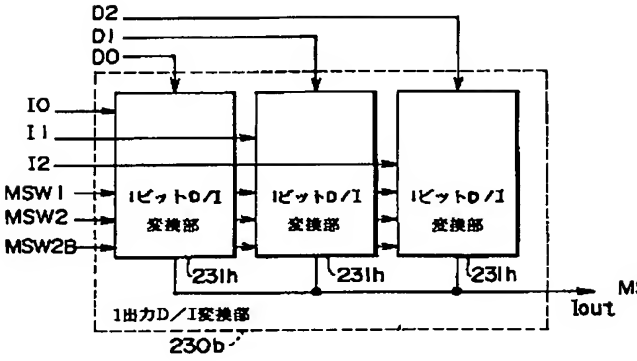
【図１８】



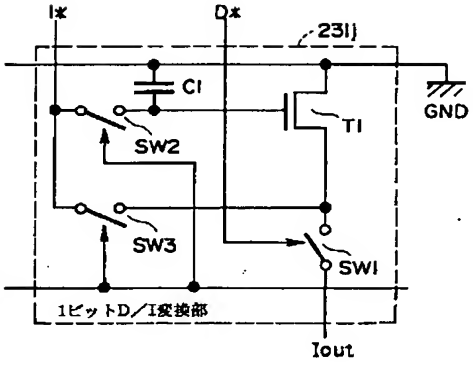
【図１５】



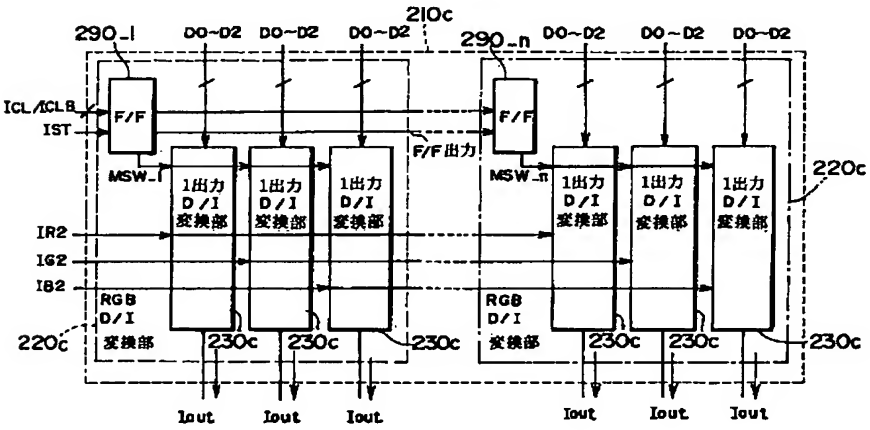
【図１６】



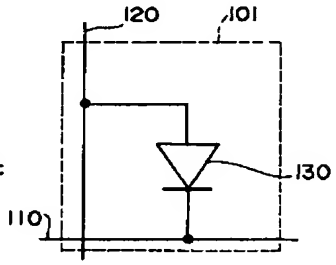
【図３０】



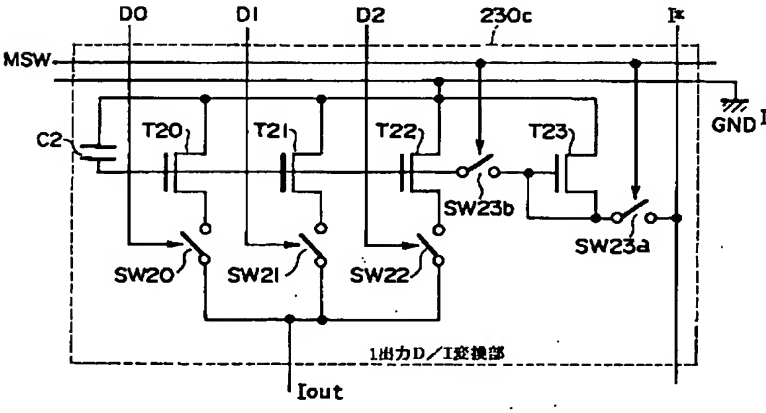
【図１９】



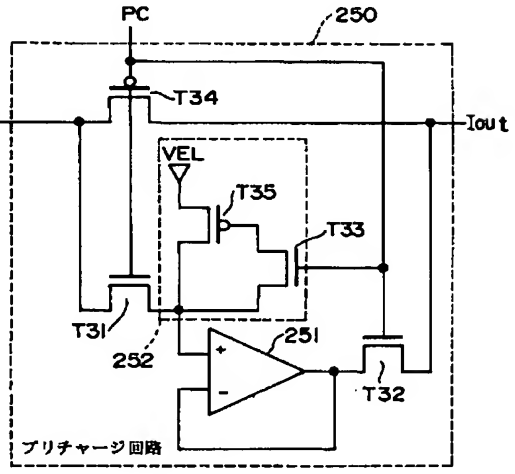
【図３６】



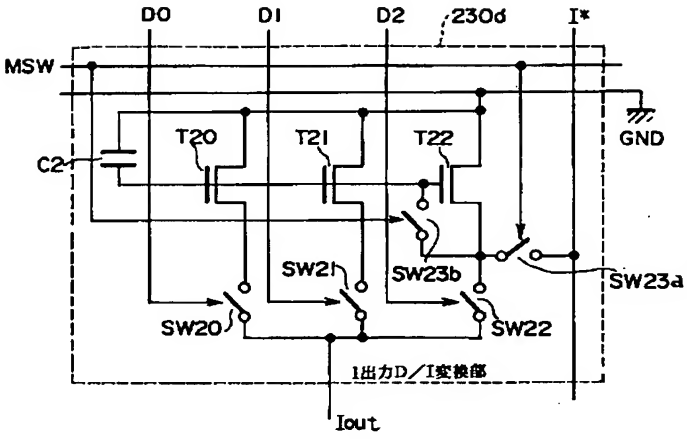
【図２０】



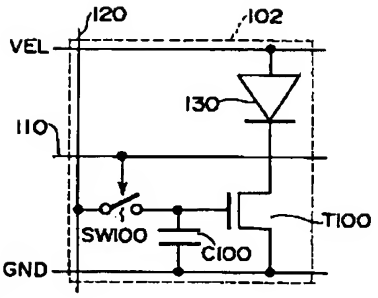
【図２７】



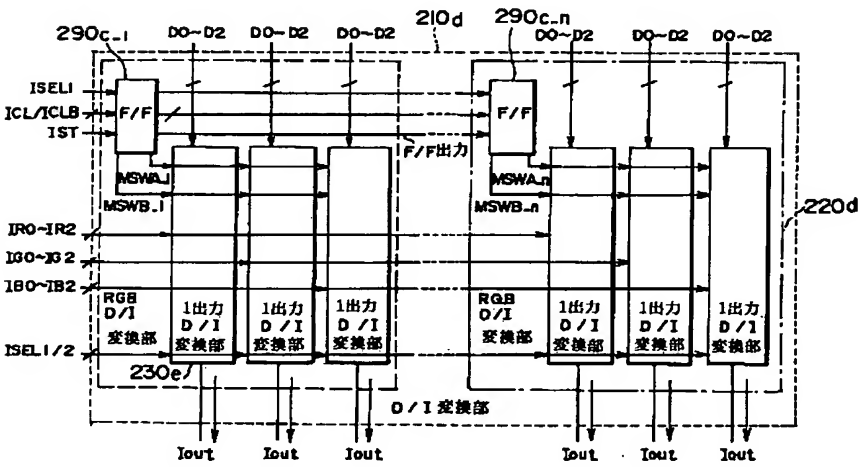
【図２１】



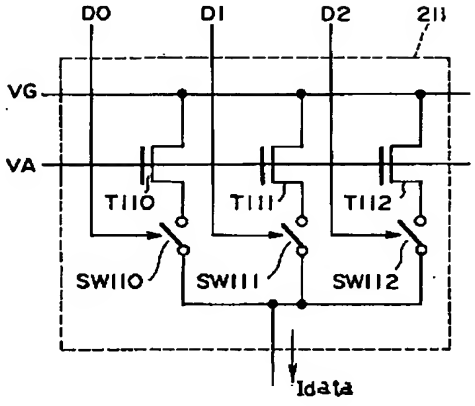
【図３７】



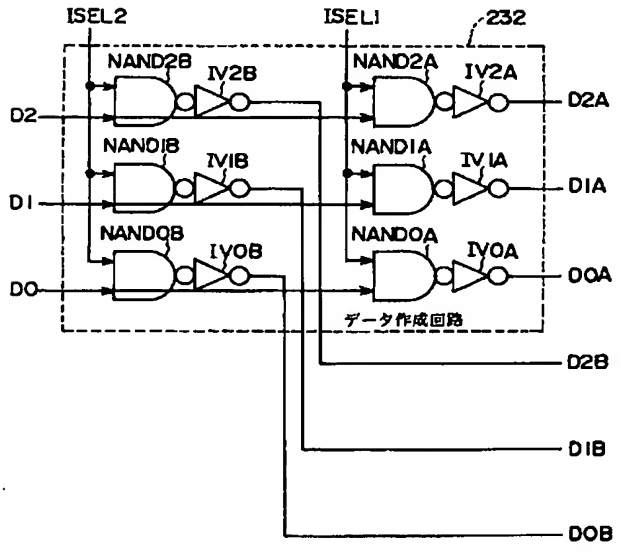
【図２２】



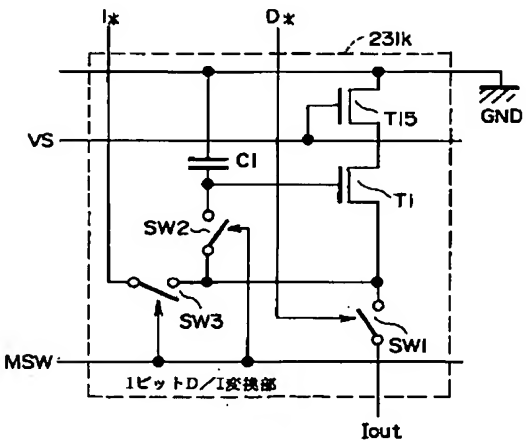
【図４０】



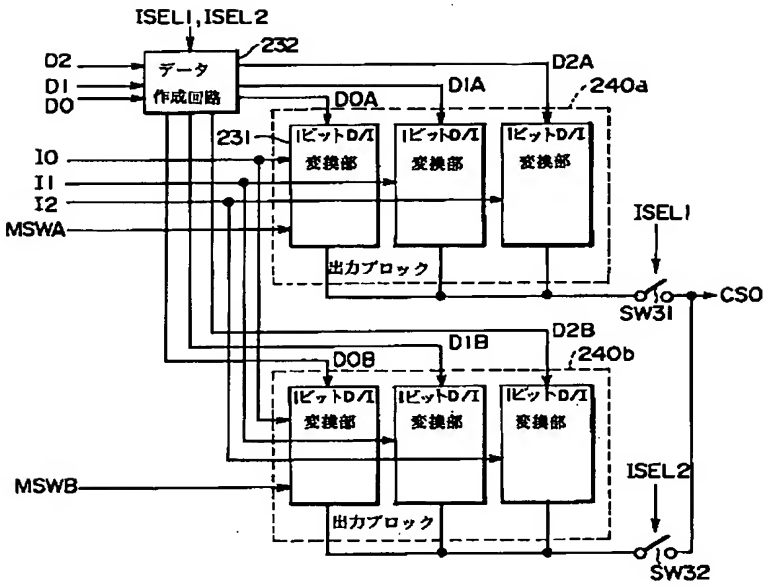
【図２４】



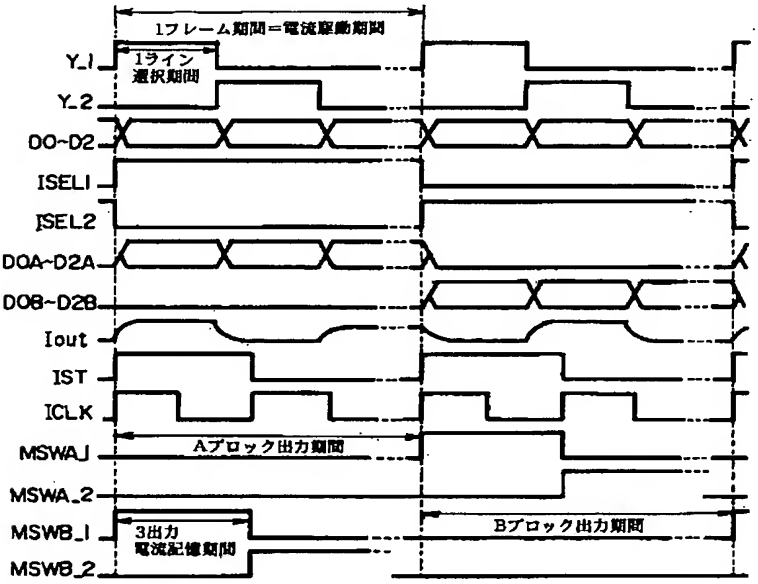
【図３１】



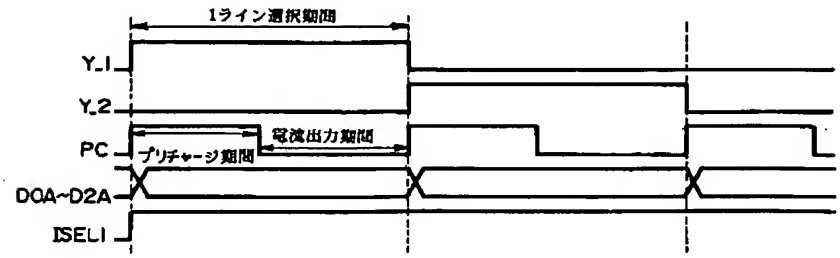
【図２３】



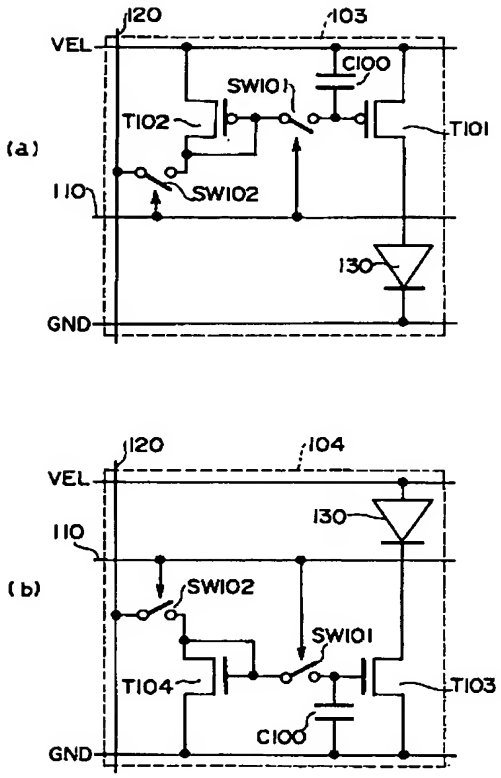
【図２５】



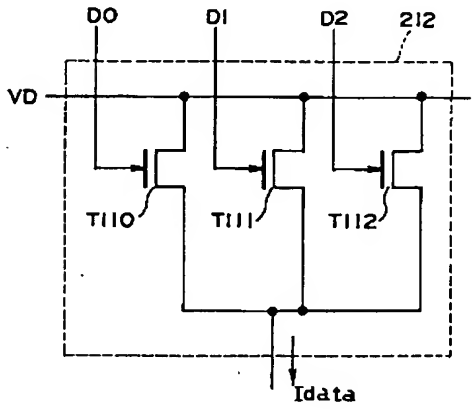
【図２８】



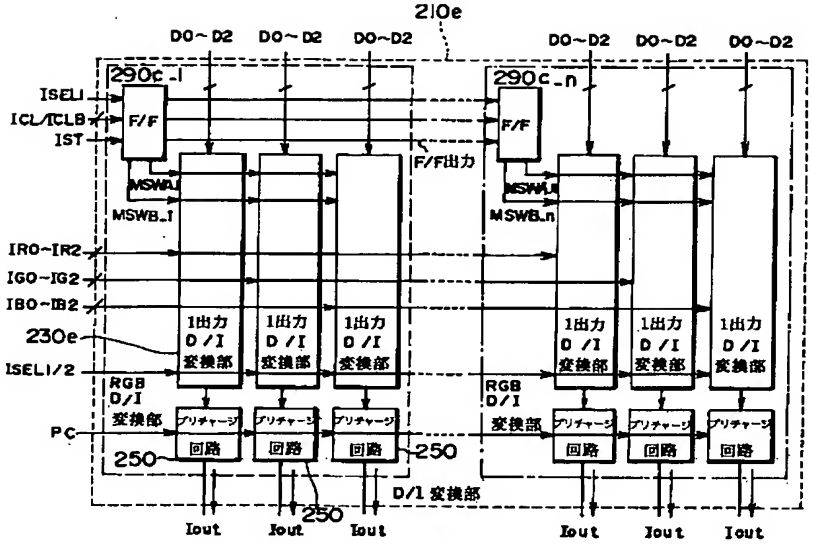
【図３８】



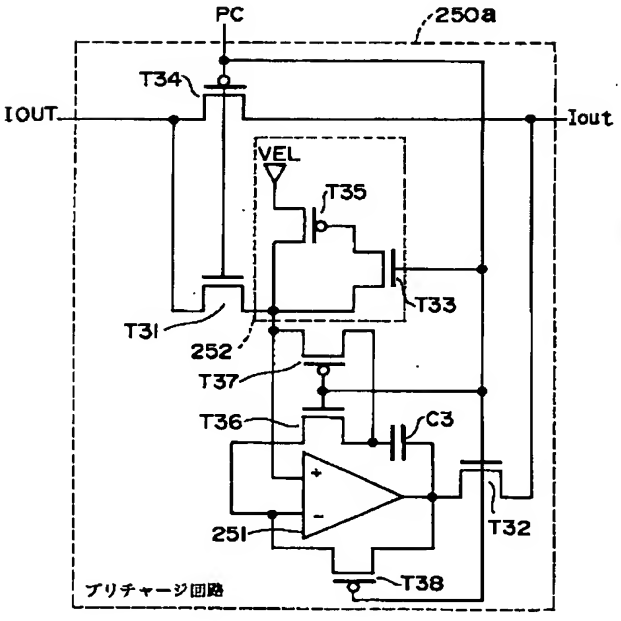
【図４１】



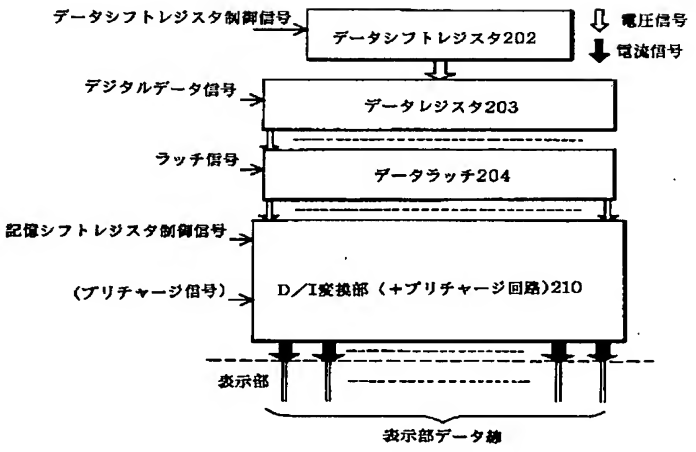
【図２６】


210e
D0~D2
290c_1
290c_n
ISEL1
ICL/ICLB
IST
F/F
F/F出力
MSWB_1
MSWB_n
IR0~IR2
IG0~IG2
IB0~IB2
230e
ISEL1/2
RGB D/I 変換部
1出力 D/I 変換部
PC
プリチャージ回路
250
D/I 変換部
Iout

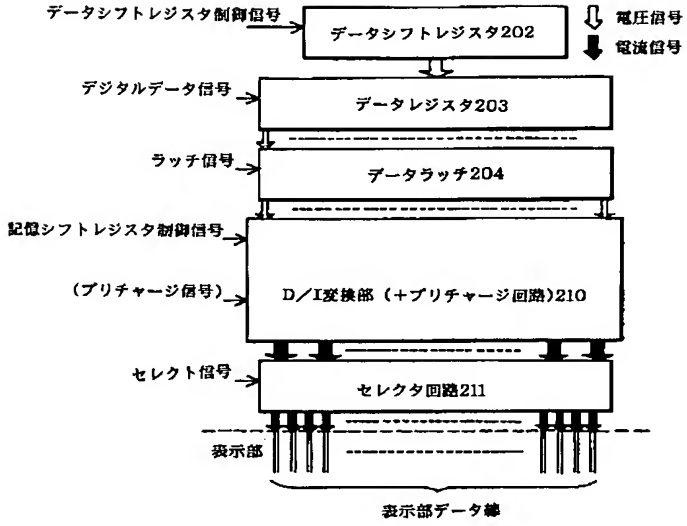
【図２９】


PC
250a
T34
IOUT
Iout
VEL
T35
T33
T31
252
T37
T36
C3
T32
251
T38
プリチャージ回路

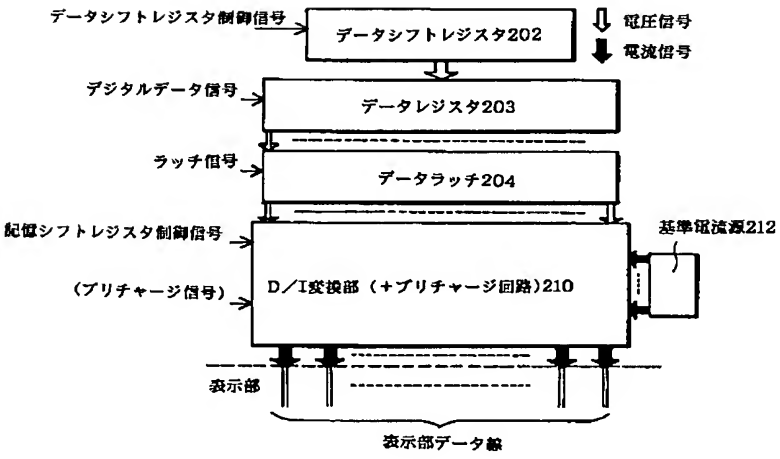
【図３２】


データシフトレジスタ制御信号
データシフトレジスタ202
電圧信号
電流信号
デジタルデータ信号
データレジスタ203
ラッチ信号
データラッチ204
記憶シフトレジスタ制御信号
(プリチャージ信号)
D/I変換部（+プリチャージ回路)210
表示部
表示部データ線

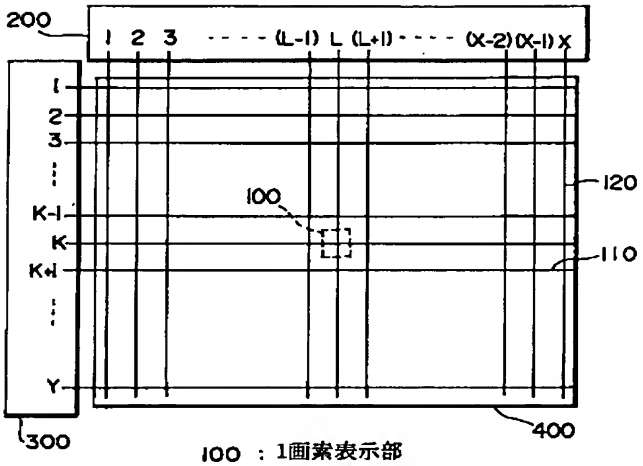
【図３３】



【図３４】

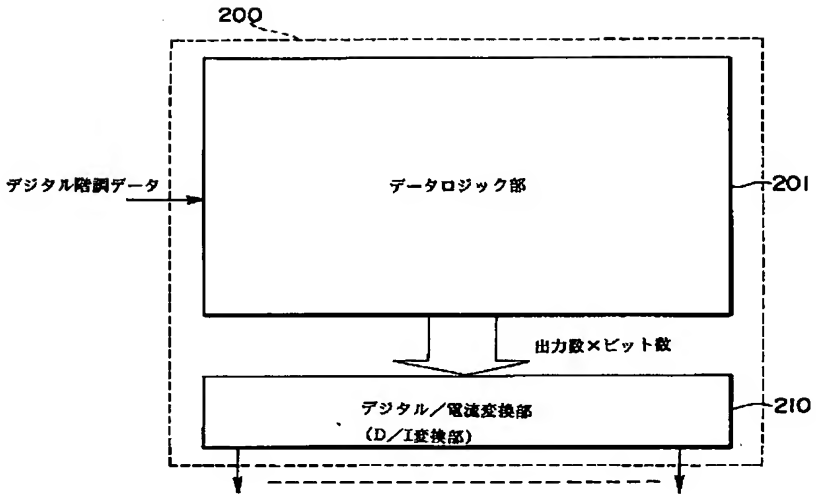


【図３５】



100 ：1画素表示部
200 ：水平駆動回路
300 ：垂直走査回路
400 ：表示部

【図３９】



フロントページの続き

(51) Int.Cl.[7]		識別記号	F I		テーマコード（参考）
Ｇ０９Ｇ	3/20		Ｇ０９Ｇ	3/20	６２３Ｆ
					６２３Ｖ
		６４１			６４１Ｄ
		６８０			６８０Ｇ
Ｈ０４Ｎ	5/70		Ｈ０４Ｎ	5/70	Ａ